Reed Business Information

EDN®

VOICE OF THE ENGINEER

JULY 10
Issue 14/2008
www.edn.com

SENSORY OVERLOAD

Page 38

BRIDGING THE NEW DISPLAYPORT STANDARD

Page 29

MEASUREMENT-BASED SIMULATION SIMPLIFIES ANALYSIS OF LOSSY BACK-PLANES AND CABLES

Page 57

DESIGNING EMBEDDED-SYSTEM APPLICATIONS WITH HIGH-LEVEL TOOLS

Page 67

The New Oscilloscope Experience Is Here

Quick Insight. Deep Insight.

Experience the New LeCroy Oscilloscopes.

www.insightwithconfidence.com

LeCroy

www.lecroy.com 1-800-5-LeCroy


America's Online
DISTRIBUTOR of CHOICE!
80.0%
60.0%
40.0%
20.0%
0%
07 Jan 2008
14 Jan
21 Jan
28 Jan
04 Feb
11 Feb
18 Feb
25 Feb
03 Mar
10 Mar
17 Mar
24 Mar
31 Mar 2008
51.36%
18.68%
17.05%
8.16%
2.12%
1.66%
0%
0%
www.digikey.com
distributor #2
distributor #3
distributor #4
distributor #5
distributor #6
distributor #7
distributor #8
© Copyright 1998-2008 Hitwise Pty, Ltd.
hitwise
An Experian company
Digi-Key CORPORATION
Quality Electronic Components, Superior Service
www.digikey.com
1.800.344.4539
701 Brooks Ave. South • Thief River Falls, MN 56701 • USA
© 2008 Digi-Key Corporation

Green Engineering

Powered by National Instruments

MEASURE IT

Acquire environmental data from thousands of sensors

Analyze power quality and consumption

Present measured data to adhere to regulations

FIX IT

Design and model more energy efficient machines

Prototype next-generation energy technologies

Deploy advanced controllers to optimize existing equipment

For more than 30 years, National Instruments has empowered engineers and scientists to measure, diagnose, and solve some of the world's most complex challenges. Now, through the NI graphical system design platform, engineers and scientists are using modular hardware and flexible software to not only test and measure but also fix inefficient products and processes by rapidly designing, prototyping, and deploying new machines, technologies, and methods. Today, a number of the world's most pressing issues are being addressed through green engineering applications powered by NI products.

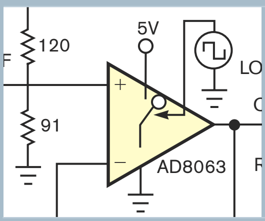
>> Download green engineering resources at **ni.com/greenengineering** **800 890 1345**

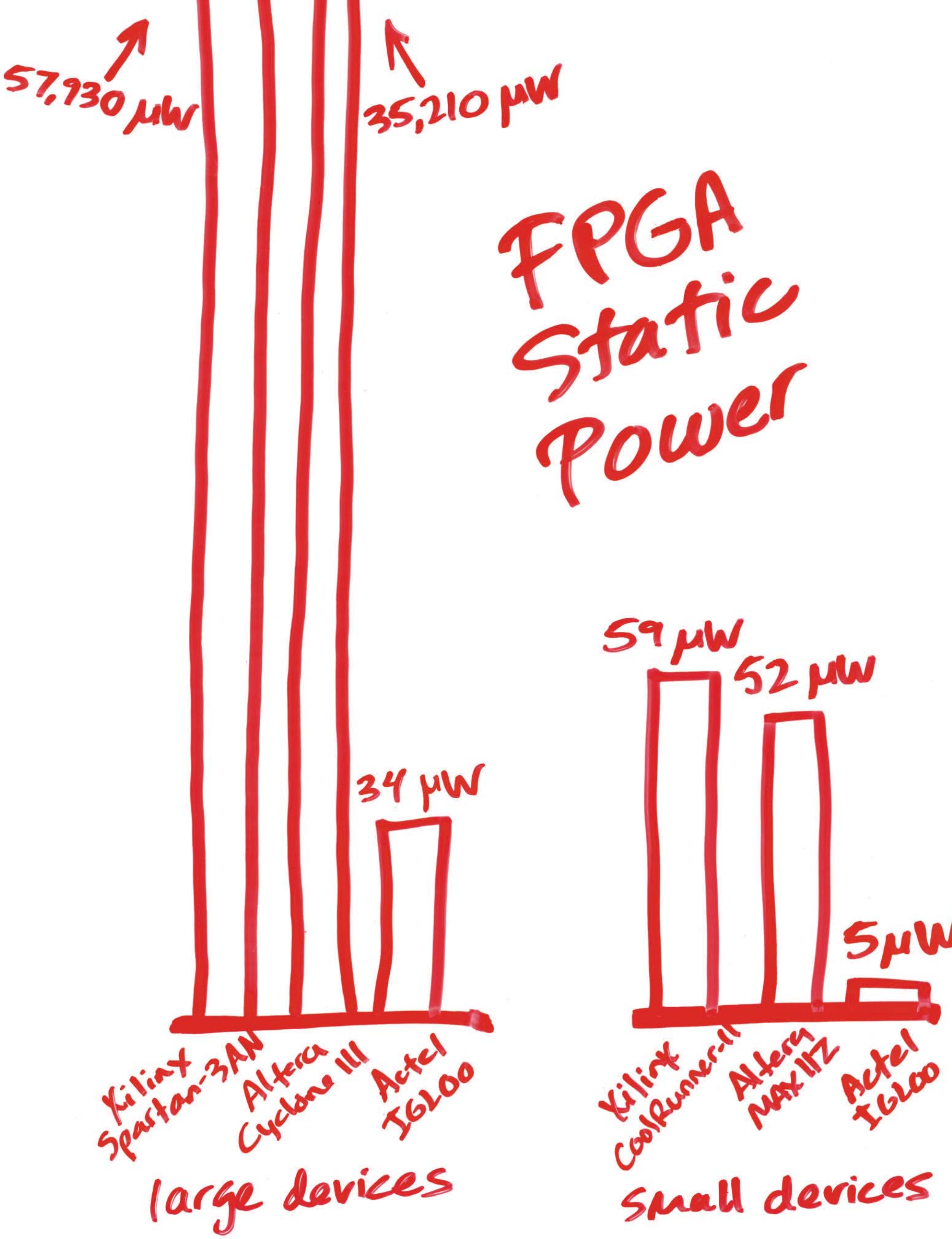
NATIONAL INSTRUMENTS™

EDN contents

7.10.08

DESIGNIDEAS





WHAT DO WE HAVE TO DO, DRAW YOU A PICTURE?

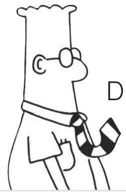
Only Actel gets you this close to zero. Any other claims of low power superiority are just that. According to their own data, Altera® and Xilinx® use between 10 and 1700 times the power of Actel IGLOO® FPGAs, depending on device and mode. Want specifics? Visit us to get the whole picture, including a video of actual measurements.

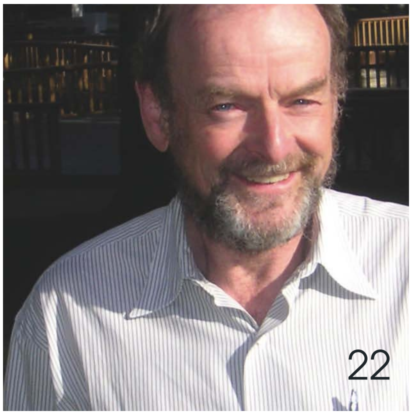
* more proof and pictures at **actel.com/power**

Actel®
POWER MATTERS

contents 7.10.08

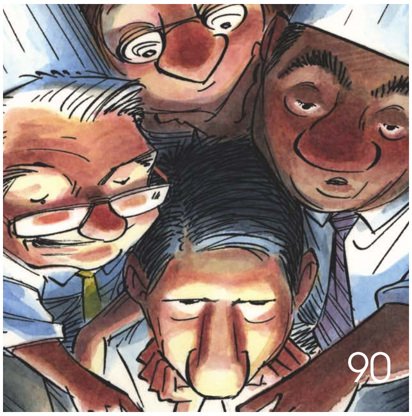
pulse





22

26

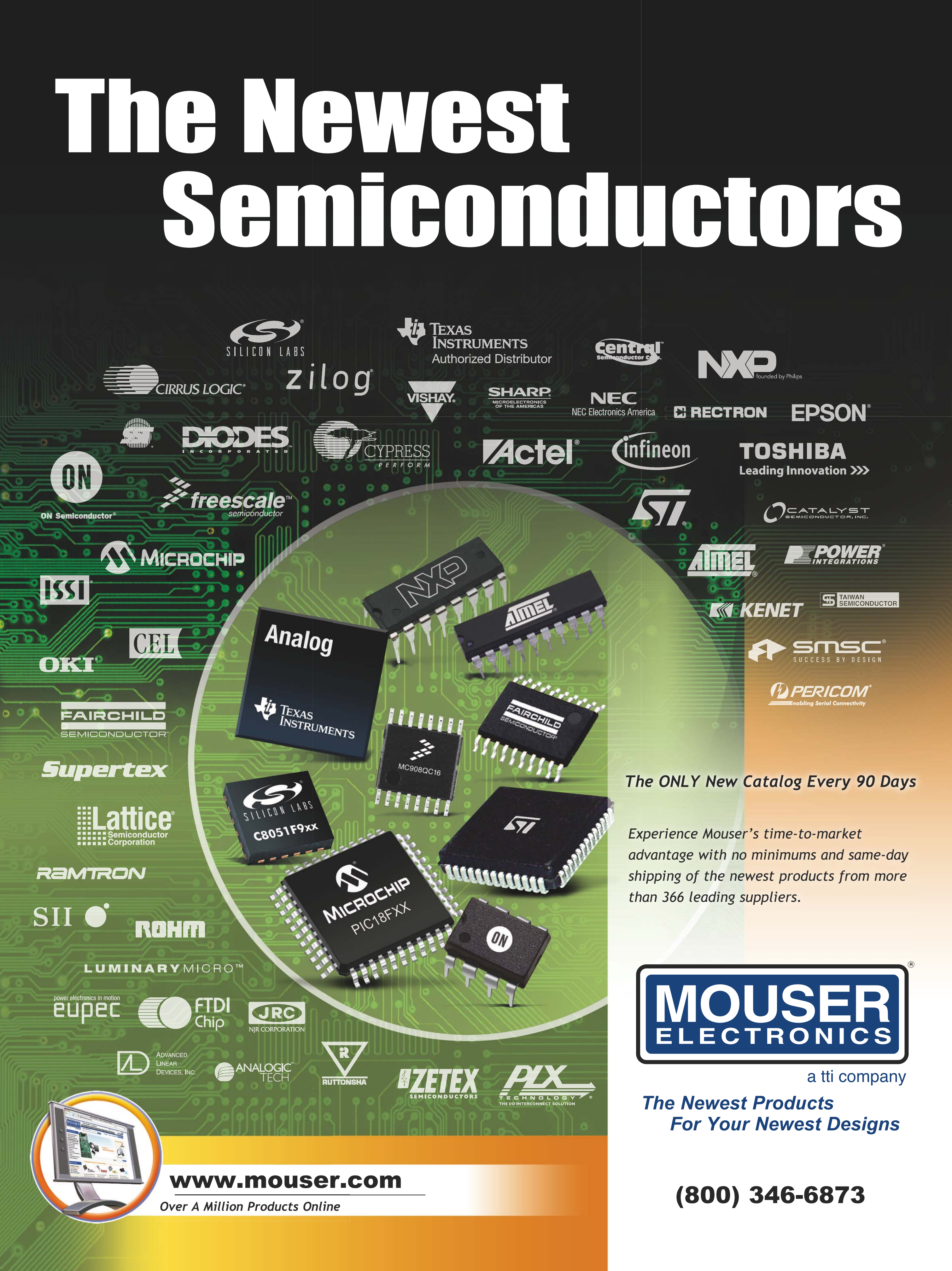


90

DEPARTMENTS & COLUMNS

PRODUCT ROUNDUP

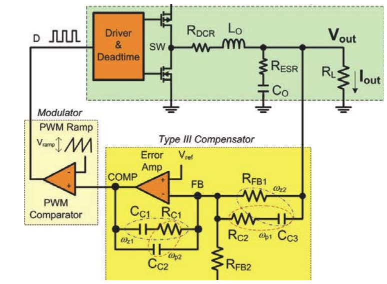
EDN® (ISSN#0012-7515), (GST#123397457) is published biweekly, 26 times per year, by Reed Business Information, 8878 Barrons Blvd, Highlands Ranch, CO 80129-2345. Reed Business Information, a division of Reed Elsevier Inc, is located at 360 Park Avenue South, New York, NY 10010. Tad Smith, Chief Executive Officer; Mark Finkelstein, President, Boston Division. Periodicals postage paid at Littleton, CO 80126 and additional mailing offices. Circulation records are maintained at Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Telephone (303) 470-4445. POSTMASTER: Send address changes to EDN®, PO Box 7500, Highlands Ranch, CO 80163-7500. EDN® copyright 2008 by Reed Elsevier Inc. Rates for nonqualified subscriptions, including all issues: US, $165 one year; Canada, $226 one year, (includes 7% GST, GST#123397457); Mexico, $215 one year; air expedited, $398 one year. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. Publications Agreement No. 40685520. Return undeliverable Canadian addresses to: RCS International, Box 697 STN A, Windsor Ontario N9A 6N4. E-mail: Subsmail@ReedBusiness.com. Please address all subscription mail to EDN®, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. EDN® is a registered trademark of Reed Elsevier Properties Inc, used under license. A Reed Business Information Publication/Volume 53, Number 14 (Printed in USA).


The Newest Semiconductors
Texas Instruments Authorized Distributor
The ONLY New Catalog Every 90 Days
Experience Mouser's time-to-market advantage with no minimums and same-day shipping of the newest products from more than 366 leading suppliers.
MOUSER ELECTRONICS
a tti company
The Newest Products For Your Newest Designs
www.mouser.com
Over A Million Products Online
(800) 346-6873

EDN online contents

www.edn.com

HOME | NEWS CENTER | DESIGN CENTERS | BUSINESS CENTERS | PART SEARCH | MORE...



ONLINE ONLY

Check out these Web-exclusive articles:

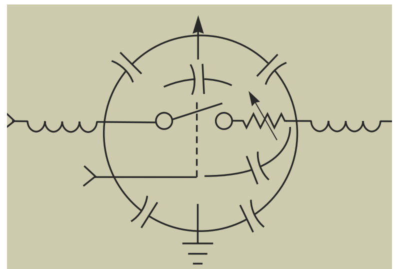
Voltage-mode control and compensation: intricacies for buck regulators
Before designing with one of today's powerful buck-regulator ICs, you'll want a thorough understanding of voltage-mode control and compensation.
→www.edn.com/article/CA6572733

Freedom of choice: harnessing the benefits of an open approach to system design
GUEST OPINION: Moving beyond a conventional IDE-based design flow can introduce a valuable expansion in the choices available to designers and provide innovative new ways to create embedded-system designs.
→www.edn.com/article/CA6570278

Battery-operated, 6.2-GHz real-time spectrum analyzer incorporates DPX technology, GPS, and mapping
Tektronix describes its latest real-time spectrum analyzer, the $22,900, rechargeable-battery-operated, 10-kHz to 6.2-GHz SA2600, as a handheld instrument.
→www.edn.com/article/CA6572715

Low-power audio codec incorporates charge pump for Class G headphone amplifier
Wolfson recently announced the low-power WM8903 audio codec for handheld consumer electronics.
→www.edn.com/article/CA6570925

Network processor integrates programmable Ethernet switch
Xelerated's next-generation HX300 network-processor family integrates traffic management and fully programmable Ethernet switches.
→www.edn.com/article/CA6570635



READERS' CHOICE

A selection of recent articles receiving high traffic on www.edn.com.

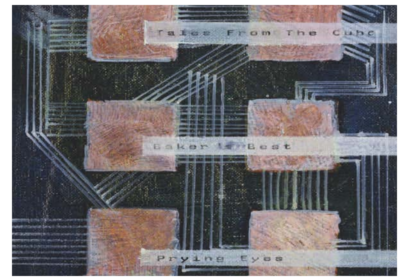
Use analog switches to multiplex your signals
Pay careful attention to analog switches and multiplexers, which are critical components of the signal path. Designers should understand the applications and specifications of these important analog parts.
→www.edn.com/article/CA6566534

Analog filter eases delta-sigma-converter design
With this "easy-to-design" circuit, you can tackle the major noise contributors around the delta-sigma modulator's sampling frequency.
→www.edn.com/article/CA6566532

Precision temperature controller has thermal-gradient compensation
An electronic work-around cancels the effects of thermal gradients in the load's thermal impedances.
→www.edn.com/article/CA6566535

Programmable current source requires no power supply
A programmable current source is useful for creating I-V curves, charging and discharging batteries, preloading power supplies, and many other applications.
→www.edn.com/article/CA6566536

Intel's Atom came with a fight
According to Intel Senior Fellow and Chief Technology Officer Justin Rattner, the chip giant took some convincing to build the low-power processor now known as Atom.
→www.edn.com/article/CA6569559



FAST ACCESS

Use these handy short cuts to access complete archives of your favorite columnists and articles on www.edn.com.

Signal Integrity
By Howard Johnson, PhD
→www.edn.com/signalintegrity

Baker's Best
By Bonnie Baker
→www.edn.com/bakersbest

Tales from the Cube
True engineering stories, as told by EEs
→www.edn.com/tales

Analog Domain
By Joshua Israelsohn
→www.edn.com/analogdomain

Tapeout
By Pallab Chatterjee
→www.edn.com/tapeout

Prying Eyes
An inside look at design decisions
→www.edn.com/pryingeyes

All technical articles
In-depth features by staff editors and contributors
→www.edn.com/features

Voices
Q&A with industry experts
→www.edn.com/voices

Analog Angle
By Ron Mancini
→www.edn.com/analogangle

BY RON WILSON, EXECUTIVE EDITOR

Where is EDA going now?

Is this the case of the vanishing electronic-design-automation industry? Early last month, the annual Design Automation Conference opened its doors to what was, by all accounts, a smaller-than-hoped-for crowd. Some vendors—notably Cadence Design Systems—were absent from the show floor, and many others were in downsized booths. There was talk that DAC had to change. At press time, Cadence had just announced an unsolicited bid for Mentor Graphics, which Mentor then promptly dismissed as too small and inadvisable for regulatory reasons. There is talk of consolidation among the three pillars of the EDA industry—Cadence, Mentor, and Synopsys—indicating the final maturing of the market.

But what is really going on? Is EDA going away? Will all chip-design tools become legacy tools? Will designers turn to open-source software? Will foundries have to create tool chains on their own to sell wafers? I think not. Rather, some important changes have been altering the EDA landscape for years, and these changes—in the geographic composition of the chip-design community and in the nature of the chip-design process—are now impossible to conceal. They will also profoundly alter the nature of the EDA industry without in any way compromising its fundamental role in the electronics industry.

First, there is the geographic element. Ever since Texas Instruments and a few other pioneers began a decade ago creating design centers in India and Taiwan, the geographic center of chip-design activity has been shifting west, across the Pacific. Industry opinion has lagged in its awareness of this shift: Many people think of advanced ICs as primarily designed in Austin, TX; Silicon Valley; or upstate New York. But many chip-design teams depend heavily on design centers in India, in Taiwan, or in mainland China. And that is where the new seats for EDA tools are.

This migration has not reached its endpoint. These Asian countries are no longer merely job shops for US or European design teams. Increasingly, whole, leading-edge fabless-chip-design teams work in Taiwan in the shadow of the giant foundries. You can find them in both India and mainland China. Estimates suggest that hundreds of fabless-chip houses in China today are doing active design work. EDA is alive and well, and it has a growing customer base. But that growth is not in North America, and it does not depend on a legacy-EDA-business model.

This fact brings up the other change: the nature of the chip-design process. In the supposed glory days of the EDA industry, EDA software had the same kind of leverage as, say, corporate-infrastructure software or PC software: You write it once, a million people buy it, and you have wonderful margins. But increasingly, EDA is not a merchant business; it is, to the horror of investors, a service business. EDA vendors don't sell stuff to their leading customers; they form multiway partnerships with their customers, with leading IP (intellectual-property) vendors, and with foundries. Vendors are still struggling to adjust their business models to this different reality on the ground, and that struggle by itself is responsible for much of the turmoil in the industry.

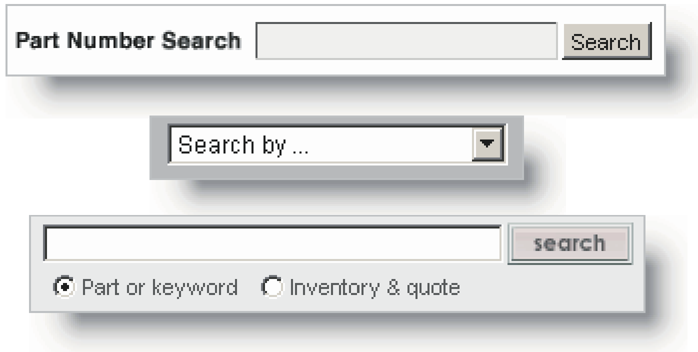
Without the leverage of an off-the-shelf software model, EDA vendors can't show huge returns on investment from license sales. It looks as if the roof is falling in. But other industries have gone through this transition. Look at IBM, which used to generate huge returns from manufacturing mainframe hardware. It now does very well, thank you, deriving much of its earnings from services contracts. And as I write this editorial, legendarily hardware-oriented computer maker Hewlett-Packard is trying to acquire IT-services-vendor EDS (Electronic Data Systems). It is possible to have strong earnings growth based on services. EDA will learn how to do it, as, by the way, will the silicon-IP business.

Is EDA maturing? No. It is entering a new growth phase, marked by a rapidly expanding customer base and even greater demands for innovation. What has ceased to grow is the legacy-business model that worked only in another time, with customers in another place. Change hurts, but change, if you understand it, can be excellent. **EDN**

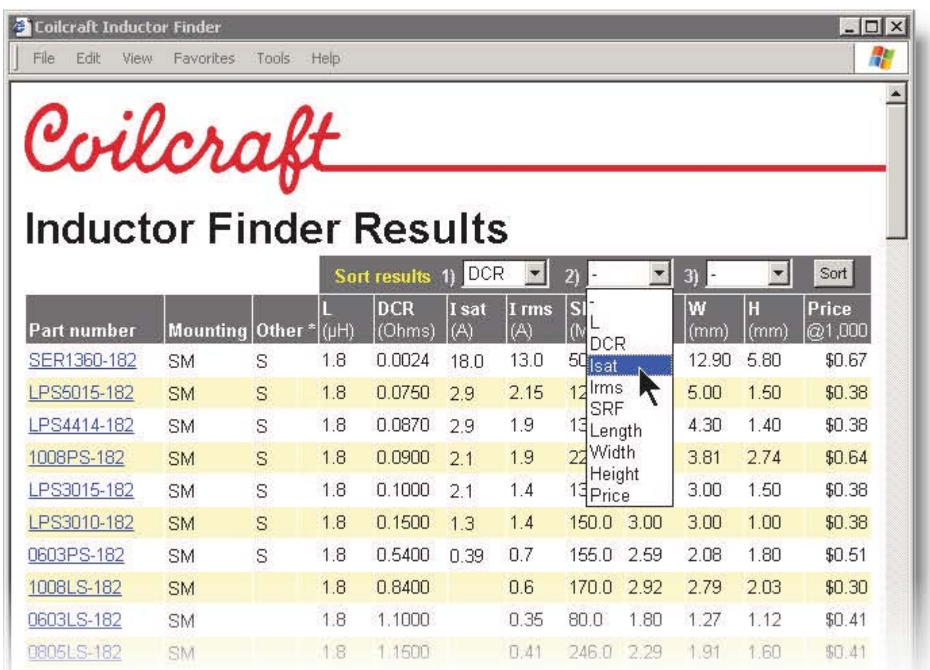
Contact me at ronald.wilson@reedbusiness.com.

MORE AT EDN.COM

+ Go to www.edn.com/080710ed and click on Feedback Loop to post a comment on this column.



Their sites have search engines. Ours has a find engine.



On most inductor web sites, their search engine results in more aggravation than answers.

But Coilcraft's web site is different.

In seconds, our Inductor Finder will show you all the parts that meet your electrical and size requirements. You can sort the results by your most important parameters. Compare pricing. Even analyze the core and winding losses of up to four different power inductors!

You'll find lots of other design tools to help you choose the perfect part. And then request free samples with just a few clicks.

So quit searching for magnetics and start finding them at **www.coilcraft.com**!

ORDER DIRECT
BUY.COILCRAFT.COM
800-322-2645
OVERNIGHT DELIVERY ORDER BY 5
RoHS COMPLIANT

Coilcraft®

www.coilcraft.com 800/322-2645

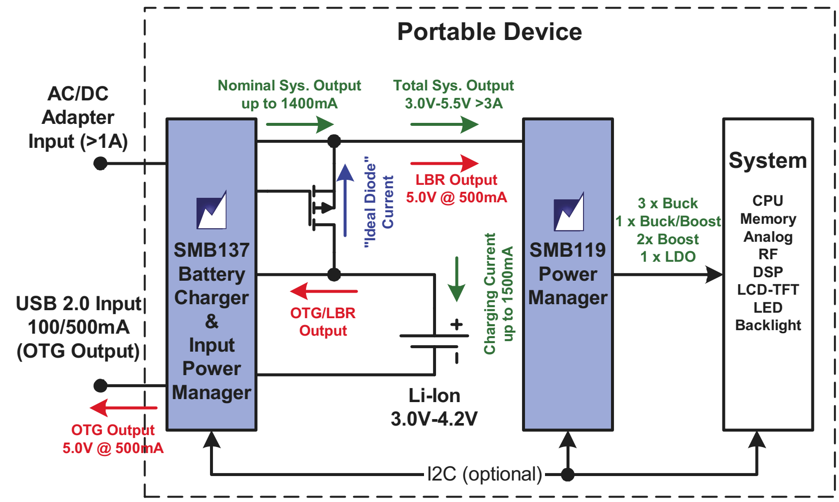
EDN

EDN. 225 Wyman St, Waltham, MA 02451. **www.edn.com**. Phone 1-781-734-8000. **Address changes or subscription inquiries:** phone 1-800-446-6551; fax 1-303-470-4280; subsmail@reedbusiness.com. For a free subscription, go to **www.getfreemag.com/edn**. Reed Business Information, 8878 S Barrons Blvd, Highlands Ranch, CO 80129-2345. Include your mailing label.

Reed Electronics Group

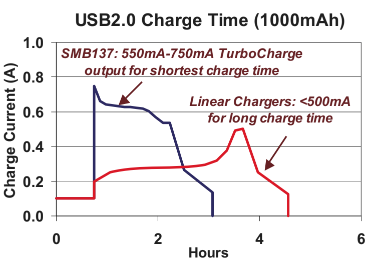
Complete PMU and Charger Solutions For Any Portable Application – No Compromises

Summit's Programmable Power and Battery Managers Provide The Best Performance, Integration and Flexibility

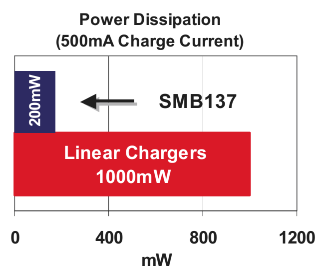


Applications

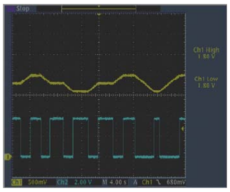
- Multimedia/Smart Phones
- MP3/MPEG4 Players/TV
- Handheld Games
- Handheld GPS Terminals
- Digital Cameras/Camcorders



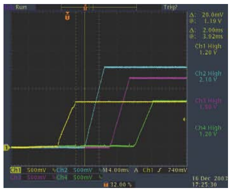
50% Faster Charging



75% Lower Power



Dynamic Output XScale™/ARM™



Sequencing

Programmable Battery Chargers

Product	SMB137	SMB138	SMB135/235	SMB139/239
Topology	Switch-mode	Switch-mode	Switch-mode	Linear-mode
Input Voltage Range (V)*	4.35 to 5.5 (16)	4.35 to 6.2 (16)	4.35 to 6.5 (10)	4.35 to 6.5 (10)
# of Inputs/Outputs	2/2	1/1	1/1	1/1
Maximum Charge Current (mA)	1500	1250	900	210/525
TurboCharge™ Output	Automatic	Automatic	Software/uC	
CurrentPath™ Control	X			
USB On-The-Go Power	X	X		
Low-Battery Recovery Mode	X			
I2C Interface	X	X	X	X
Programmable Algorithm	X	X	X	X
UV/OV/Thermal/Timer Safety	X	X	X	X
Package	3.6x3.3 CSP-30	3.1x2.1 CSP-20	2.1x1.3 CSP-15	2.1x1.3 CSP-8
Total Solution Size (mm2)	50	28	31	7.5

* () Indicates maximum input overvoltage "holdoff"

Programmable Power Managers

Product	SMB122	SMB119	SMB118	SMB113
Total # of Outputs	9	7	7	4
Step-down (Buck)	3 or 4	3 or 4	3 or 4	4
Step-up (Boost)	2 or 4	2 or 3	1 or 2	
Inverter (Buck-Boost)	0 or 1			
Battery Charger	1		1	
LDO	1	1	1	
Package Size (mm)	9x9	7x7	7x7	5x5

For more information see:

www.summitmicro.com

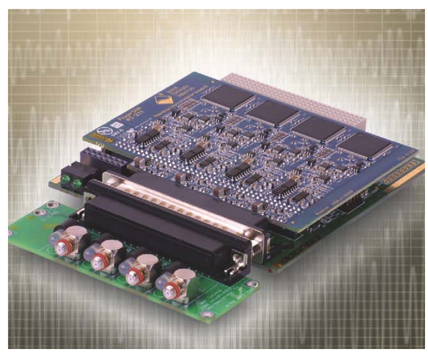
Featuring MobileGreen™ Technologies
www.summitmicro.com/MobileGreen

SUMMIT MICROELECTRONICS
Programmable Power for a Green Planet™

Interface module captures acceleration, vibration data

The latest analog-input board from United Electronic Industries features four isolated accelerometer/vibration-sensor channels with sample rates to 125k samples/sec per channel, 24-bit resolution, and 109-dB SNR (signal-to-noise ratio). The DNA-AI-211 allows direct connection to industry-standard, IEP (integral-electronics-piezoelectric), two-wire vibration sensors and provides both software and LED annunciation of open or shorted sensors.

A combination of analog and digital FIR (finite-impulse-response) filters provides the board's 100-dB digital antialiasing filtering. The digital filter allows a combination of a passband ripple of ±0.005 dB, steep falloff, and a stop-band floor of −100 dB, which are unattainable figures with simple analog filtering. The digital nature of the filter also ensures that each filter induces an identical phase shift, so no filter-induced interchannel phase jitter will impact or corrupt subsequent analysis. The factory provides support for Windows, Linux, and VxWorks operating systems; several programming languages; and application packages, such as LabView, Matlab, and DasyLab. Prices for the DNA-AI-211 start at $2000, and it is available from stock.**—by Warren Webb**



The four-channel DNA-AI-211 vibration-sensor-interface board features 125k-sample/sec sample rates, 24-bit resolution, and a 109-dB SNR.

▷**United Electronic Industries**, www.ueidaq.com.

FEEDBACK LOOP

"Ah, history repeats itself! Some 30+ years ago, I taught an audio class that necessitated adjusting trimpots while watching an analog meter. One of the big worries of the day was that these 'kids' didn't know the difference between turning the pot clockwise or counterclockwise.

—Reader Barry Ober, in *EDN*'s Feedback Loop, at www.edn.com/article/CA6562587. Add your comments.

Microcontroller interfaces ARM7 core with FPGA

Atmel's ARM7 (www.arm.com)-based AT91CAP7E microcontroller includes an FPGA interface, a six-layer AHB (advanced high-speed bus), a peripheral-DMA controller, and 160 kbytes of on-chip SRAM. The FPGA interface includes direct access to two AHB masters, four AHB slaves, the peripheral-DMA controller, and a programmable ROM to remap the external RAM to emulate and debug ROM code.

Atmel provides FPGA logic to encode and decode the bus traffic that flows between the FPGA and the CAP7E microcontroller. The logic blocks in the FPGA connect to the CAP7E through the AHB master and slave channels. The priority-interrupt controller supports as many as 13 encoded interrupts and two unencoded interrupts for DMA transfers. On-chip peripherals include a USB 2.0 full-speed device; master and slave SPIs (serial-peripheral interfaces); two USARTs; three 16-bit timer counters; an eight-channel, 10-bit ADC; and a full-function system controller, including interrupt- and power-control and supervisory functions.

The customizable CAP7 has a metal-programmable block with 450,000 gates, or the equivalent of 56,000 FPGA logic cells. You can directly migrate FPGA functions to a CAP7 device with no special EDA tools or customer-side engineering. Standard FPGA-software tools support implementation of functions such as LCD controllers, DSP algorithms, and proprietary customer IP (intellectual property). The AT91CAP7E uses the same development tools as the AT91SAM ARM-based microcontrollers, and it is available now for $9.50 (10,000) in a 225-ball BGA package.

—by Robert Cravotta

▷**Atmel**, www.atmel.com.

QorIQ moves Power architecture to multicore

Freescale's QorIQ next-generation PowerQUICC (quad-integrated-communications-controller)-processor line provides a migration path for embedded-multicore designs. The platform includes single-, dual-, and many-core devices that employ the e500 Power architecture. The first three of the planned five QorIQ processor families will be available for general sampling in 2009. Prices for the P1 and P2 products start at $23 and $50 (volume quantities), respectively.

The QorIQ P1 and P2 platforms comprise five package-, pin-, and software-compatible processors with single- or dual-core-processing options and operating from 400 to 800 MHz, targeting networking, telecom-line applications, and base-station-channel cards with thermal constraints. The QorIQ P1and P2 platforms include a 256- or 512-kbyte L2 cache that you can configure as SRAM or stashing memory. The integrated security engine supports security algorithms, such as IPSec (Internet Protocol security), Kasumi, and VPNs (virtual private networks). The memory controller supports both DDR2 and DDR3 memory and error-correcting codes. The integrated interfaces include SERDES (serializer/deserializer), GbE (gigabit Ethernet), USB, and PCIe (peripheral-component interconnect express). The P1 series offers an encryption accelerator, and the P2 series integrates RapidIO.

> Each processor can perform an independent boot and reset.

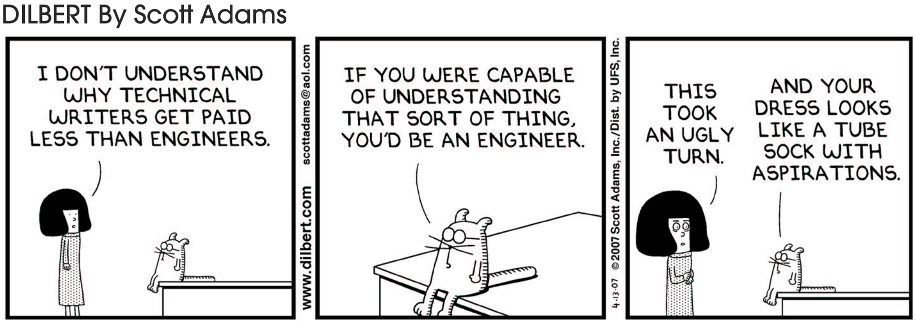
The QorIQ P4 platform includes the P4080 multicore processor that integrates eight e500mc cores operating as fast as 1.5 GHz with a trilevel-cache hierarchy, CoreNet on-chip fabric, and datapath acceleration that supports active operation within a 30W maximum-power envelope. The cores can work as eight SMP (symmetric-multiprocessing) cores, eight AMP (asymmetric-multiprocessing) cores, or a combination of both. Each processor can perform an independent boot and reset. The CoreNet fabric boosts performance by avoiding bus contention, bottlenecks, and latency issues associated with shared-bus/shared-memory architectures. The datapath-acceleration architecture manages packet routing, security, QOS (quality of service), and deep-packet inspection. The QorIQ P4080 features dual XAUI (10-GbE-attachment-unit-interface) controllers, eight 1-Gbps GbE SGMII (serial-gigabit-media-independent-interface) controllers, three PCIe Version 2.0 controllers/ports operating as fast as 5 GHz, and two serial-RapidIO 1.2 controllers/ports operating as fast as 3.125 GHz.

The QorIQ P4080 has an embedded "hypervisor" that ensures that software running on any core can access only the resources that it is explicitly authorized to access. The hypervisor includes a peripheral-access-management unit, which provides address translation and access control for all bus masters in the system. Freescale has partnered with Virtutech (www.virtutech.com) to create a hybrid simulation environment that combines Virtutech's Simics fast-functional model with a detailed performance model of the QorIQ P4080 processor. Before the emergence of first silicon, developers have a deterministic environment in which they can see and control variables without real-world-hardware constraints.

—by Robert Cravotta

▷**Freescale**, www.freescale.com.

DILBERT By Scott Adams



07.10.08

8-BIT I²C-BUS EXPANDER HAS LOW STANDBY CURRENT

Catalyst Semiconductor's new, 8-bit CAT9534 GPIO (general-purpose-input/output) expander connects to a system through an I²C (interintegrated-circuit) serial bus. The expander, targeting I²C and SMBus-based systems, is pin-for-pin compatible with the industry-standard CAT9554 but uses 100 times less standby power, consuming a maximum of only 1 μA. The eight ports power up as inputs, and you can then configure them as outputs by writing to an internal register. The device features an external power-on-reset feature to eliminate any glitches on power-up. Each port can sink 25 mA and source 10 mA. When you configure the ports as inputs, they are compatible with 2.5, 3.3, and 5V logic levels. The unit operates on 2.3 to 5.5V and is compatible with the 400-kHz I²C bus.

The CAT9534 is available in 16-pin SOIC, TSSOP, and 4×4-mm TQFN packages for 83 cents (10,000) and operates at −40 to +85°C. —by Paul Rako

▶Catalyst Semiconductor, www.catsemi.com.

The CAT9534 bus expander provides eight I/Os from a 400-kHz I²C bus or SMBus.

Flexis adds EMC/EMI support to microcontroller family

Freescale's Flexis AC family of microcontrollers, the third member of the Flexis series, adds support for quiet EMC (electromagnetic-compatibility)/EMI (electromagnetic-interference) performance to both the 8- and the 32-bit devices. The family targets motor-control and human-machine interfaces for white-goods applications, such as washing machines and refrigerators, as well as general industrial applications, such as factory automation, building control, and HVAC (heating/ventilation/air-conditioning) systems. The microcontrollers maintain the same pin-, peripheral-, and software-compatible architecture as the other Flexis members, and the family acts as a migration path for Freescale's 8-bit MC9S08AW designs.

The 8-bit S08AC128/96 Flexis AC devices feature a 40-MHz S08 core with a 10-MHz system bus that supports as much as 8 kbytes of SRAM and as much as 128 kbytes of flash memory with an operating range of 2.7 to 5.5V. The devices include three TPMs (time/pulse-width modulators); a 10-bit, 16-channel ADC; an internal clock generator; and independently clocked COP (computer-operating-properly) and CRC (cyclic-redundancy-check) counters.

The devices also include as many as two SPI (serial-peripheral-interface), two SCI (serial-communications-interface), and I²C (interintegrated-circuit)-bus interfaces in 44-pin LQFP, 64-pin QFP, and 64-pin LPFP packages. Samples are available now, and prices for the S08AC128 start at $2.48 (10,000).

The 32-bit ColdFire devices support operation as fast as 50 MHz with a 25-MHz system bus and as much as 32 kbytes of SRAM and 256 kbytes of flash memory operating with a single supply voltage of 5V. The devices include a CAN (controller-area-network) bus; the ability to synchronize the 12-bit, 24-channel ADC; and a 16-bit Flex timer module. Safety features support the IEC (International Electrotechnical Commission) 60730 Class B regulation, and additional features include active power-on reset, low-voltage detection, and low-voltage warning. The devices support independently clocked COP and CRC counters and as many as two SPI, two SCI, and I²C-bus interfaces in 64-pin LQFP, 64-pin QFP, and 80-pin LQFP packages. Samples are available now, and prices for the MCF51AC256 start at $3.54 (10,000).

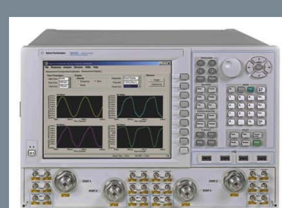
A complimentary Version 6.1 CodeWarrior development studio for microcontrollers and the Processor Expert tool support development for the Flexis AC microcontrollers. Freescale offers the DemoACkit evaluation system for the Flexis AC family. It contains the 8- and 32-bit Flexis AC daughtercards and a built-in USB BDM (background-debugger mode), LEDs, a serial port, an acceleration sensor, and an I/O header. The DemoACex expansion board plugs into the DemoACkit and allows developers to take advantage of integrated features, such as the CAN. The DemoACkit is available for $99, and the DemoACex kit is available for $30.

—by Robert Cravotta

▷**Freescale**, www.freescale.com.

VNA ANALYZES ACTIVE-DEVICE NONLINEAR BEHAVIOR

Agilent Technologies has announced NVNA (nonlinear-vector-network-analyzer) capability for its PNA-X microwave-network analyzer, which operates from 10 MHz to 26.5 GHz. Requiring minimal external hardware, the Agilent NVNA software effectively converts a four-port PNA-X into a high-performance nonlinear analyzer. Featuring nonlinear-component characterization, nonlinear-pulse-envelope-domain capabilities, and support for nonlinear parameters that Agilent calls X parameters, the new capability targets R&D engineers and scientists researching and designing active-RF components.



Agilent's nonlinear-vector-network analyzer measures the calibrated amplitude and cross-frequency-relative phase of measured spectra from 10 MHz to 26.5 GHz, including the fundamental, harmonics, and cross-frequency products.

The instrument's new X-parameter support extends linear S-parameter-measurement capability into the nonlinear operating region and enables an accurate portrayal of both nonlinear-device and cascaded-nonlinear-device behavior using measurement-based data. You can use the X parameters in Agilent's Advanced Design System software to simulate and design using nonlinear components, modules, and systems.

One of the NVNA's key capabilities is its ability to measure the calibrated amplitude and cross-frequency relative phase of measured spectra from 10 MHz to 26.5 GHz, including the fundamental, harmonics, and cross-frequency products. As a result, engineers can better understand and control the nonlinear behavior of their devices under test. The unit can display data in the time, frequency, power, or user-defined custom domains, providing additional insight into the nonlinear behavior of components.

The NVNA also provides a nonlinear-pulse-envelope-domain measurement, which enables researchers to gain a deeper understanding of the memory effects their devices exhibit by displaying harmonic-pulse envelopes. The NVNA can display both the amplitude and the phase of the pulse in the time domain, which shows the changes over time. The base price for the nonlinear-support option for the N5242A PNA-X microwave-network analyzer is $56,000.—by Rick Nelson

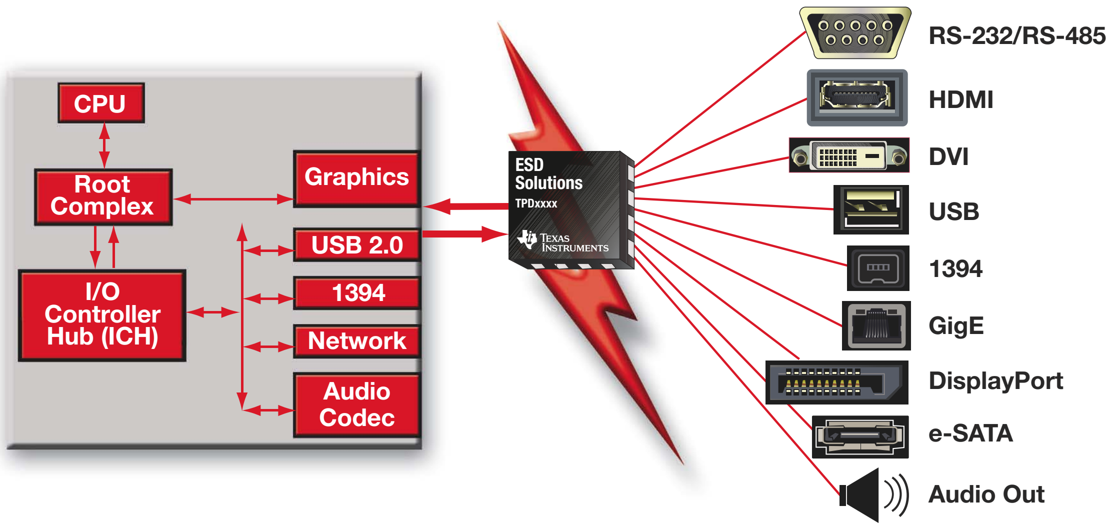
▶**Agilent Technologies, www.agilent.com.**

07.10.08

System-Level ESD Protection Devices

Space-saving, low capacitance solutions

High-Performance Analog>>Your Way™



System-level ESD strikes are a constant threat to device reliability and functionality. Many low-voltage core chips only offer device-level, human-body model (HBM) ESD protection, which doesn't address the system-level risks. TI's TPD family of stand-alone ESD devices provides space-saving and cost-effective solutions to protect the system interconnects from external ESD strikes. For multiple external interfaces including video, audio and serial data transfer, the TPD family offers IEC61000-4-2 level ESD protection.

Device	# Channels	Supply Voltage (V_{DD})	I/O Level (V)	I/O Capacitance (PF)	V_{BR} (min) (V)	Package	Application
TPD2E001	2	0.9-5.5	0-V_{DD}	1.5	11	SOT-5, SON-6	USB 2.0, RS-232 / RS-485
TPD3E001	3	0.9-5.5	0-V_{DD}	1.5	11	SOT-5, SON-6	USB OTG
TPD4E001	4	0.9-5.5	0-V_{DD}	1.5	11	SOT-6, SON-6	USB 2.0, Ethernet, Firewire, e-SATA, RS-232 / RS-485
TPD6E001	6	0.9-5.5	0-V_{DD}	1.5	11	QFN-10, QFN-12	USB 2.0, Ethernet, Firewire, e-SATA, RS-232 / RS-485
TPD4E004	4	0.9-5.5	0-V_{DD}	1.6	6	SOT-6, SON-6	USB 2.0, Ethernet, Firewire, e-SATA
TPD6E004	6	0.9-5.5	0-V_{DD}	1.6	6	QFN-8	USB 2.0, Ethernet, Firewire, e-SATA
TPD4S009	4	0.9-5.5	0-V_{DD}	0.9	9	SOT23-6, SC70-6, SON-6	e-SATA, LVDS signaling
TPD8S009	8	0.9-5.5	0-V_{DD}	0.9	9	SON-15	HDMI, DisplayPort
TPD12S520	12	0.9-5.5	0-V_{DD}	0.9	9	TSSOP-38	HDMI receiver port
TPD12S521	12	0.9-5.5	0-V_{DD}	0.9	9	TSSOP-38	HDMI transmit port

www.ti.com/esd 1.800.477.8924 ext. 4498
Get samples and datasheets

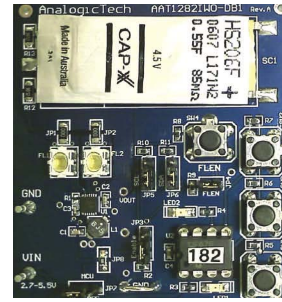
Texas Instruments

Supercapacitor powers LED flash

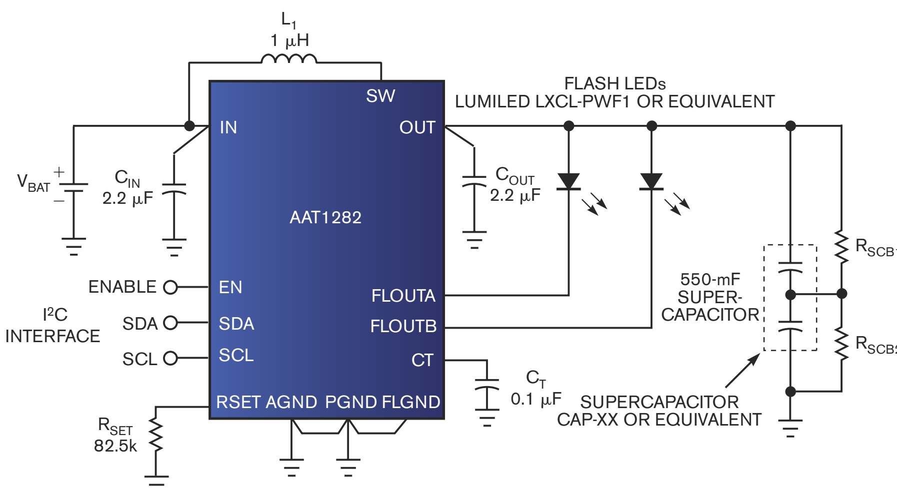
Advanced Analogic Technologies has introduced a 2-MHz boost-converter IC that uses a supercapacitor to provide a large peak current to an LED-flash system. The 2A AAT1282 flash driver incorporates I²C (inter-integrated-circuit) control and accepts input voltages of 2.7 to 5.5V. Designers can use the device's two 1A current sinks to drive two LEDs and can parallel these outputs to drive one 2A LED. The IC allows designers to set 16 levels for movie, or "torch," mode and has a true-load-disconnection feature that guarantees a shutdown current of less than 1 μA. The device achieves 90% efficiency with a 1-μH inductor.

Using a supercapacitor to provide for a reservoir of current, the product protects the battery from high-discharge events and allows LED brightness approaching that of a xenon flash. The 0.55F supercapacitor comprises two 2.5V capacitors so that the IC can always operate in boost mode. The circuit also includes 2.2-μF ceramic capacitors to reduce ac-circulating currents, yielding lower EMI (electromagnetic-interference) emissions and ensuring that current from the supercapacitor doesn't flow back into the battery.

The AAT1282 is available in a 14-pin, 3×3-mm, TDFN (thin-dual-inline-flat) package with a suggested retail price of $1.75 (1000). The IC operates across a −40 to +85°C temperature range. Samples and evaluation modules are available now.**—by Paul Rako**
▷**Advanced Analogic Technologies**, www.analogictech.com.



The AAT1282 evaluation board provides a starting point for engineers developing LED-flash applications.

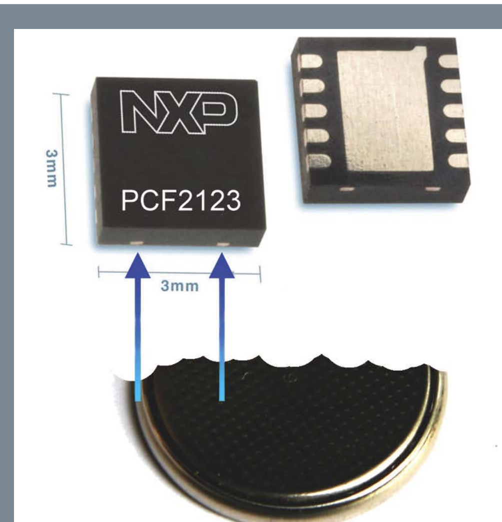


The AAT1282 boost-converter IC transfers energy from a cell-phone battery to a supercapacitor to achieve 2A LED-flash currents.

ULTRALOW-POWER REAL-TIME CLOCK EXTENDS BATTERY LIFE

NXP Semiconductor's PCF2123 real-time clock has an operating current of less than 100 nA, or 0.15 μW, on a 1.5V power supply. The 3×3×1-mm package includes a freely programmable alarm-and-timer function that can generate a wake-up signal on an interrupt pin. A programmable offset register supports fine-tuning of the clock and frequency adjustment.

The seconds, minutes, hours, days, weekdays, months, and years registers are coded in BCD (binary-coded-decimal) format. Data from the real-time clock is accessible serially through an SPI (serial-peripheral-interface) bus with a maximum data rate of 6.25 Mbps. The CMOS-based device uses a low-power, 32.768-kHz quartz oscillator that you can calibrate using an on-chip calibration register. The device requires no other external parts. The PCF2123 real-time clock is available now for 55 cents (high volumes).—by Robert Cravotta
▶**NXP Semiconductor, www.nxp.com.**



The PCF2123 real-time clock measures 3×3×1 mm and has an operating current of 100 nA.

VOICES

National Semiconductor's David Anderson

David I Anderson is chief technologist for power management at National Semiconductor. He has spent a long and distinguished career in the electronics business and often provides unique insights on the various panels and forums he participates in as a technology guru. *EDN* asked Anderson about his past, present, and future.

I notice an accent; where were you born?

A My father briefly worked in England around the time I [was born]. We returned to Alloa [Scotland], where I grew up with my four brothers, attending Dollar Academy and Edinburgh University.

What was your first job after leaving school? Was it what you expected?

A My first job at Nuclear Enterprises was to assist a more senior designer in developing a portable X-ray spectrometer for a mineralogy application. After Nuclear, I joined Ferranti Electronics in Edinburgh. [Later], I decided the future was in semiconductors, so I joined Siemens in Munich, Germany.

Why did you join National Semiconductor?

A At Siemens, it seemed that, whenever I completed a design, I would open a journal and see a similar product advertised from a company called National Semiconductor. The final straw occurred when I was preparing an article on camera ICs and found an ad for a new electronic-timer IC with an integrated photodiode, designed by Dennis Monticelli at National. At National in Greenock, Scotland, I developed audio ICs, including analog-telecom and Dolby ICs.

Eventually, you left National. Where did you go?

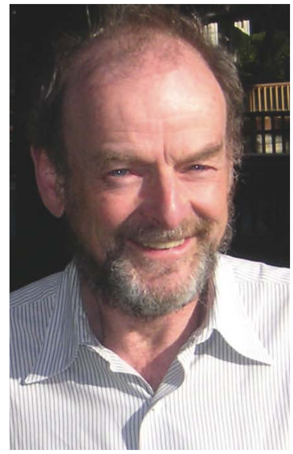
A In 1996, I joined a little-heard-of company called Semtech. [Then], I discovered a small start-up, Volterra. I joined Volterra to head up its design activities.

What market was Volterra trying to penetrate?

A The company pioneered the provision of I^2C [interintegrated-circuit]-bus access on a switcher. Volterra was one of the first companies to discern the shift from single-brick supplies to POL [point-of-load] IC regulators.

In 2004, you came back to National Semiconductor. Should National pursue digital power?

A Digital-power management is present on numerous chips available from National and others using I^2C and other bus standards. Digital-control loops present somewhat more of a challenge, but they, too, will become commonplace as topologies move below 0.18 micron. However, there is far more hype in the trade press than in the marketplace, and the ROI [return on investment] is not yet there. The customer wants a power supply that works efficiently. He does not care how we implement the control—analog or digital. The real benefits of digital are reprogrammability and time to market, particularly for multiple-output switchers. National's PowerWise technology is a particularly effective form of digital control.



"The customer wants a power supply that works efficiently. He does not care how we implement the control—analog or digital."

Can you tell us about what the future holds for the power groups and National?

A Power management has come a long way since the advent of the Simple Switcher back in 1995, yet, amazingly, there is still huge potential for further development; many exciting technologies and new applications are appearing all the time. National is blessed with many outstanding engineers, and not only in design groups. These folks are being given a sincere invitation and opportunity to innovate. Still, it is an unmistakable fact that much of the innovation in the field still comes from universities and start-ups that ultimately become partners or pieces of larger companies. We have a strategy and the talent and expertise, and we are poised for growth.

What is the biggest issue facing the users of power and power-management ICs?

A Energy and its effective management.

You joined a Silicon Valley start-up. Were there any other risks you wish you had taken?

A I suppose I have often taken risks in my career but have been very fortunate in their outcome. But the greatest risks not undertaken have been business ideas I didn't follow up on. I should really do something about that; I still have a few.

When you left Volterra, your financial status may have allowed you to retire. What drives your passion to contribute to the semiconductor industry rather than go fishing?

A I have neither the patience for fishing nor the talent for golf. And the semiconductor world is pretty stimulating most of the time. The real story, however, is that I don't feel I have made my mark.—**by Paul Rako**

BY BONNIE BAKER

"Muxing" around with delta-sigma converters

A multiplexer in your circuit can scan through a number of input channels by sampling each channel in rotation. As a power and cost advantage, multiplexed systems have only one ADC that acquires the data from all of the channels. Before starting your design, first look at the types of signals you are trying to digitize. For instance, if you know the highest and lowest frequency as well as the accuracy requirements in all of your system's channels, you may see a need for several ADCs.

In another scenario, the channels may have a unique time relationship to each other, requiring a simultaneously sampling approach that preserves phase information. You achieve this goal with sample-and-hold circuits and a single ADC, or it may be easier to use individual ADCs.

Figure 1 shows a delta-sigma converter multiplexed circuit with the antialiasing filters on the signal side of the multiplexer. Each channel of this circuit has a near-dc signal at the input of the multiplexed converter. However, a channel-to-channel change can create a step-response signal to the ADC. Thus, it is critical that you use a zero-cycle-latency converter.

Cycle latency is equal to the number of complete data cycles between the initiation of the input signal conversion and the availability of the corresponding output data. The converter must be able to generate a fully settled output signal from a step input. If the device completes the conversion before the start of the second cycle, the cycle latency is zero. One possible limitation of multiplexed delta-sigma ADCs is a nonzero cycle latency.

Figure 2 shows the signal-chain dynamics of a multiplexed system with three signals. This system links slices from each input channel. After the multiplexer, the zero-latency delta-sigma ADC sees this merged waveform, which has large and fast transitions as the signal switches from channel to channel. The reaction of the delta-sigma converter's digital filter to the entire multiplexed waveform means that the fast transitions settle completely within the digital filter.

The appropriate delta-sigma-converter class for multiplexed applications performs the conversion task with a zero-cycle-latency characteristic. These delta-sigma converters usually have sinc (sinx/x) digital filters. This class of converter masks internal-digital-filter results from a designer's view. With a zero-cycle-latency delta-sigma ADC, the first output-data results fully settle.

You can also describe a zero-cycle-latency ADC as having single-cycle settling or a single-cycle conversion. In all cases, however, you will get the right answer from the multiplexed converter the first time. **EDN**

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

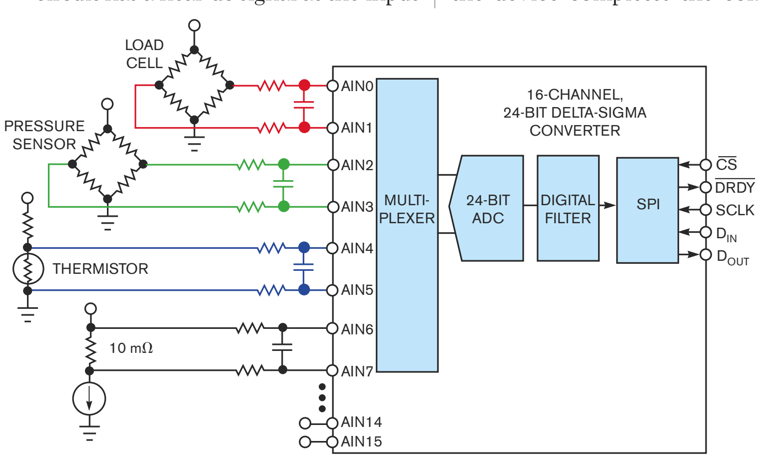


Figure 1 The signal's frequency content at the input delta-sigma converter is usually slow-moving.

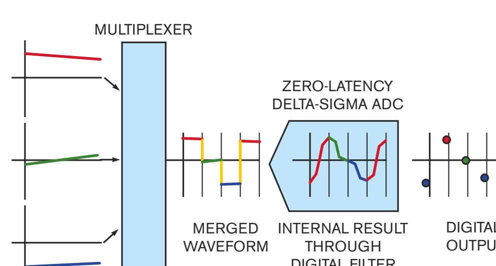


Figure 2 Switching dc signals into the ADC's input can contain high-frequency components.

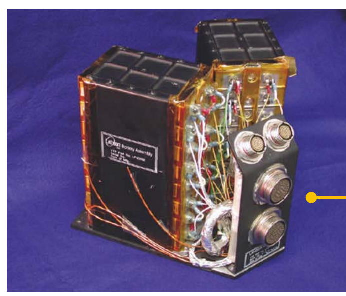
PRY FURTHER AT EDN.COM
Go to www.edn.com/pryingeyes for past Prying Eyes write-ups.

Way, way off the grid: powering the Phoenix Mars lander

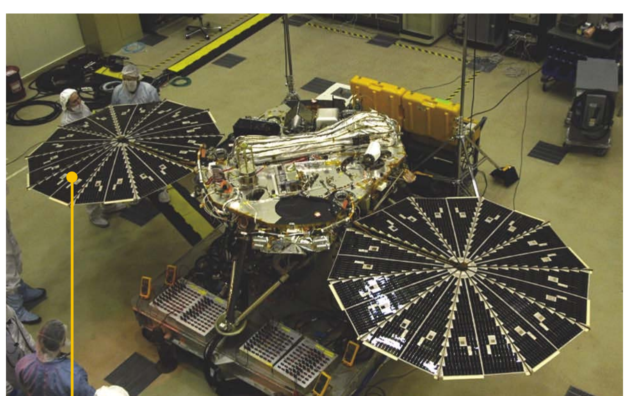
The Phoenix lander's 90-day mission at the Mars pole is to gather dirt and rock samples with its robotic arm, analyze the samples with onboard instruments, and communicate results and respond to commands with its earthbound project engineers. All of these tasks require electrical power. The power-generation, -regulation, and -delivery system for the Phoenix comprises a lithium-ion-battery pack from Yardney Technical Products and two solar arrays from ATK Space Systems.

The oncoming Martian winter constrains the mission to a tight, 90-day window. Temperatures then drop to the point at which the atmosphere, which is more than 95% carbon dioxide, freezes solid and shrouds the lander in dry ice. The Phoenix will then shut down for the winter—and, most likely, forever.

Each array unfolds like an oriental fan into a circular shape 2.1m in diameter and can generate 770W of power from sunlight at the distance Earth is from the sun. Because Mars is approximately 1.5 times farther from the sun, the solar arrays will produce less than half the power possible on Earth.

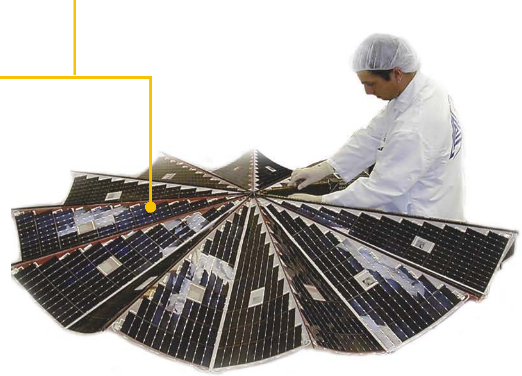


The lithium-ion battery comprises two identical battery modules as well as the electronics to monitor cell voltages, control charging and discharging, and perform cell balancing. The two modules form a V shape measuring 13.38×10×9.5 in. and weighing 17.8 kg. Each module's maximum continuous-output current is 12A at 28.8V, with an ampere-hour capacity of 33 Ahr and an energy-storage capacity of 950.4 Whr.



The Phoenix batteries will provide power at night when there is no sunlight for the solar panels to convert to electricity. The lander can also use the batteries whenever a task requires more power than the solar arrays can deliver. The battery fits inside a thermal enclosure, insulation surrounding it, on the component deck on the underside of the lander.

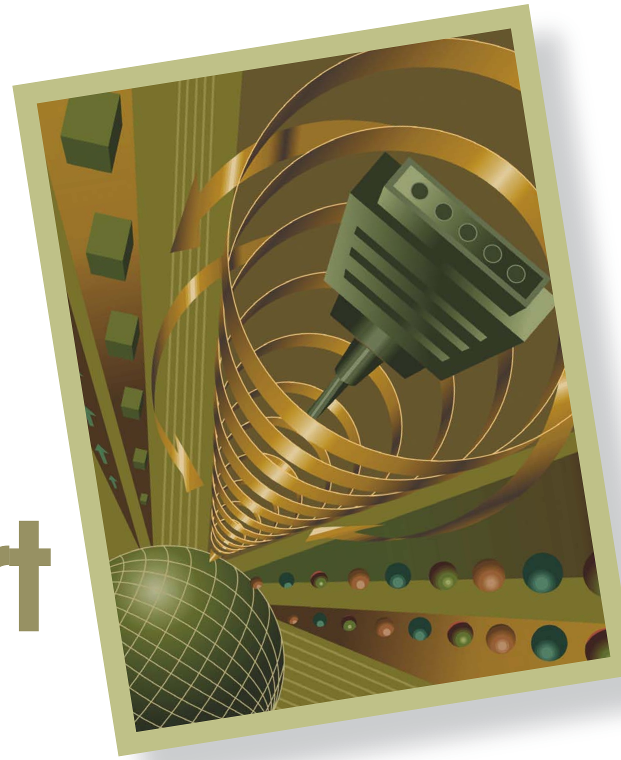
Solar arrays are the primary power source for the lander. The arrays' gallium-arsenide crystalline-photovoltaic cells have an efficiency of 27%. Developers grew the cells on a germanium substrate and then bonded them to a flexible substrate structure. The cells have the maximum photovoltaic-conversion efficiency available given the spectral content of sunlight on the Martian surface.



Just how cold does it get at the poles during a Martian winter, when the carbon dioxide atmosphere freezes solid? The atmospheric pressure fluctuates but, at its highest, is 100 times less than Earth's, where the freezing temperature of carbon dioxide is −78.5°C at 1 atm (atmosphere) pressure. At Mars' lower atmosphere, carbon dioxide freezes at −125°C (−193°F).


F-35
AA-1

DEVELOPERS OF THE NEW DISPLAYPORT STANDARD DESIGNED IT FOR EFFICIENCY. HOWEVER, DISPLAYPORT'S PARTITIONING DIFFERS FROM THAT OF TMDS-BASED ARCHITECTURES, AND ENGINEERS NEED APPROACHES FOR BRIDGING DISPLAYPORT WITH THE EARLIER HDMI AND DVI STANDARDS.



Bridging the new DisplayPort standard

BY ABDULLAH RAOUF • PERICOM

VESA (Video Electronics Standards Association) defined the emerging DisplayPort standard as an attractive alternative to digital-display-interface incumbents, such as HDMI (high-definition multimedia interface) and DVI (digital-video interface). As with any new standard, the designers of DisplayPort focused on improving some aspects of HDMI and DVI for certain applications. However, simply being more efficient in some instances is not enough for a new standard to overtake a more established interface. Although DisplayPort may be more practical from a technological and cost perspective for some applications, HDMI is already in use in a wide range of consumer-electronics devices. And, although displays for commercial PCs may migrate quickly to DisplayPort, the need to connect to HDMI-based consumer-electronics devices will result in the need to support multiple interfaces for some time. The challenge for engineers, then, will be in implementing efficient bridging that minimizes the impact on system complexity and cost.

DISPLAYPORT SPECIFICATION

You can divide the reasons for implementing DisplayPort into technological and market factors. Among the technological factors are increased capacity, consolidation of external and internal display interfaces, and smaller connectors. From a marketing perspective, DisplayPort avoids the royalties associated with HDMI, and you can efficiently implement it on smaller process technologies. It also shifts the cost from the display to the video/graphics source.

DisplayPort supports single-lane transfer rates as fast as 2.7 Gbps across as many as four data pairs for a maximum of 10.8 Gbps over a single cable. These features combine with support for color depth as great as 16 bits per color channel to give designers the option of improving image quality in applications that require screen resolution of as much as WQXGA (wide-quad-extended-graphics array), or 2560×1600 pixels, as well as increasing refresh rates to 120 Hz. The DisplayPort interface also carries embedded clock signals and provides a bidirectional auxiliary channel operating at 1 Mbps to enable link management and device control to comply with VESA's EDID (extended-display-identification) and MCCS (monitor-control-command-set) standards. This bidirectional signal allows the display to request stronger signal quality if the received signal has too much jitter or ISI (intersymbol interference). This unique design scheme allows for automatically adjusting pre-emphasis from the source. The direct-feedback path between the display and the source also allows systems to automatically fine-tune themselves for different resolutions, refresh rates, and color depths. It also provides head room to support the continued innovation that video and gaming applications drive.

With its high bandwidth, embedded

clock, and adaptive-pre-emphasis capabilities, DisplayPort can also replace internal display buses, such as the LVDS (low-voltage-differential-signaling) interfaces within notebook PCs. In addition, DisplayPort has significantly smaller connectors and channels than those of conventional LVDS-based display interfaces. For example, including the differential auxiliary channel, a one-lane DisplayPort interface uses only four wires, and a full-bandwidth, four-lane interface requires only 10. In comparison, TMDS (transition-minimized-differential-signaling)-based laptops using an 18-bit panel use a 16-line LVDS interface comprising six differential data lines and two differential clock lines, whereas 24-bit LCD panels require 20 lines.

The primary drivers for DisplayPort, in many cases, are market-based. HDMI, for example, has had sufficient time to establish itself as the digital-display interface of choice within a variety of consumer-electronics applications. To compete with HDMI and DVI, DisplayPort must provide significant benefit to trigger migration. DisplayPort attempts to lower display-interface costs in a number of ways. First, it avoids the royalties associated with HDMI standards. DisplayPort also consolidates drive circuitry within the video source using direct-drive technology similar to the technology that the original VGA (video-graphics-array) interface used. Through direct drive, DisplayPort technology eliminates the need for scaling circuitry within the monitor that costs approximately $5 to $10. As a display's PCB (printed-circuit board) is one of the limiting factors in determining its overall depth, the elimination of scaling enables the production of monitors as thin as ½ in. This feature is a key differentiator with consumers. This shifting of cost is of interest in the corporate-PC market because the higher-priced item, the PC, must absorb the scaling cost. In contrast, in the consumer-electronics market, the more expensive monitor absorbs the cost, and the DVD players and cameras are less expensive.

AT A GLANCE

- The need to connect to HDMI (high-definition-multimedia-interface) and DVI (digital-video interface) will result in the need to support multiple interfaces for some time.
- Designers are implementing the DisplayPort for both technological and market reasons.
- As DisplayPort reaches the market for chip sets moving to 45-nm processes, engineers will need a way to bridge DisplayPort and DVI.
- Bridges present an opportunity to improve signal quality through a variety of signal-enhancement techniques.

On the PC side, primary manufacturers of graphics-chip sets are driving the adoption of DisplayPort. These manufacturers include Intel (www.intel.com), AMD (www.amd.com), and Nvidia (www.nvidia.com), each of which is developing DisplayPort-based silicon. Video processing is a computationally intensive activity, and silicon vendors continue to drive down die size to minimize current consumption and increase transistor count and clock rate. However, as designers move to 45-nm and smaller processes, the inherent limitations of the process technology have a greater influence on system architecture.

For example, moving to a 45-nm process imposes a 2.5V maximum for I/O transistors. Both HDMI and DVI employ TMDS technology, so they require 3.6V when running high-speed signals and as much as 5.25V for low-speed sideband signaling. As a result, you cannot integrate TMDS-based interfaces into ICs using 45-nm-process technology without also introducing specialized and proprietary design measures that increase die size, complexity, and cost. Additionally, any expenses you incur in enabling the use of higher-voltage transistors will increase the cost of not only the electrical portion of the TMDS interface, but also the graphics-chip set onto which you integrate it. High-speed DisplayPort electrical signals, in contrast, never rise higher than 2V, so you can implement them in a standard 45-nm process without requiring special measures or introducing new architectural limitations. This characteristic plays an important role in implementing efficient bridging between HDMI/DVI and DisplayPort.

BRIDGING DISPLAYPORT

Whenever new standards are in a position to compete, it can be difficult to determine which, if any, will eventually dominate the market. Although applications exist for which DisplayPort can provide higher quality or bring significant cost savings to bear, engineers must balance these features against the market reach of HDMI and DVI. The life cycle of interface migration has many precedents. For example, when PCIe (peripheral-component interconnect express) first appeared on the scene, AGP (accelerated graphics port) was the dominant graphics-board interface, and graphics chips came with AGP interfaces. To connect their designs to PCIe-based devices, engineers used AGP-to-PCIe bridges. As PCIe gained dominance, it became the native interface, and PCIe-to-AGP bridges emerged.

As DisplayPort reaches the market

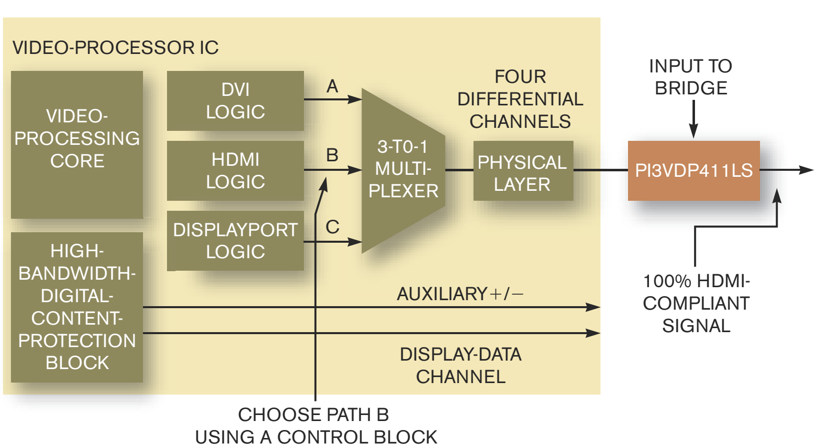
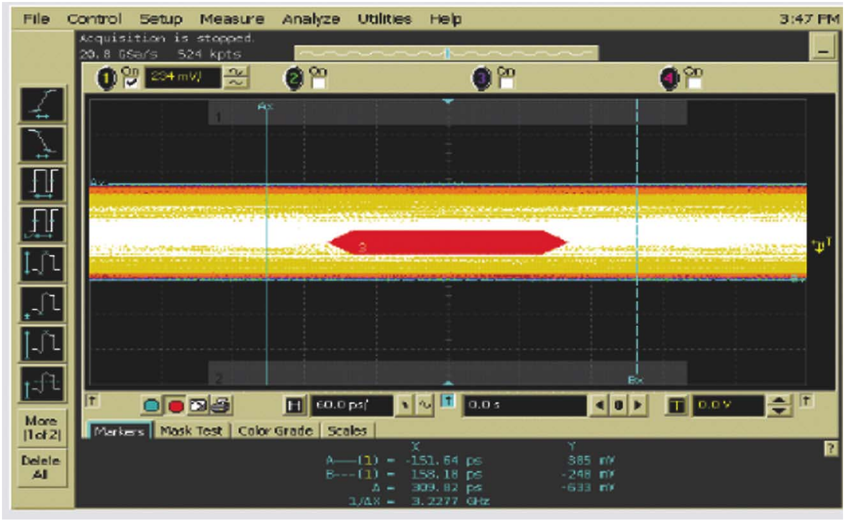
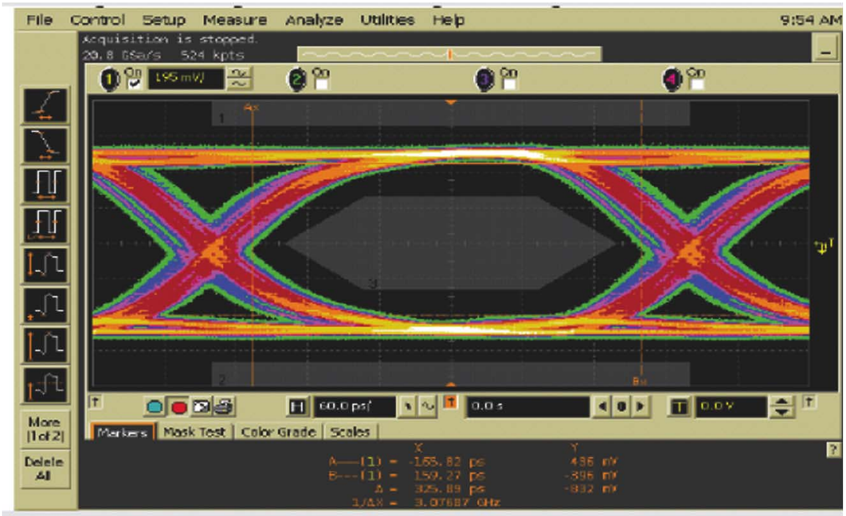


Figure 1 To facilitate efficient bridging, you use an internal multiplexer to select the appropriate logical protocol and then transmit it over a DisplayPort electrical signal. To connect to an HDMI or DVI monitor, an external bridge converts the DisplayPort electrical signal to HDMI or DVI. The conversion is then complete because it encapsulates the appropriate logical protocol.



(a)



(b)

Figure 2 The Pericom PI3VPD411LS DisplayPort-to-HDMI bridge can improve signal quality and provide higher eye margin through well-established signal-enhancement techniques, such as equalization and pre-emphasis, giving designers more freedom in board layout and connector placement. In the input to the bridge, the signal has a completely closed eye (a). Passing through jitter-elimination circuitry restores the quality of the signal at the output of the bridge (b).

for graphics-chip sets moving to 45-nm processes and, consequently, native DisplayPort interfaces, engineers will need a way to bridge to HDMI and DVI. However, even if a system uses a native DisplayPort monitor, it will most likely need to also support the HDMI and DVI interfaces of the consumer-electronics devices to which users want to connect. Because interfaces comprise both physical and logical components, engineers can design efficient bridging that separately implements each component in the most cost-effective process technology, depending on the IC within which you integrate it. From a physical standpoint, you implement the high-voltage-I/O transistors that generate HDMI and DVI electrical signaling in a 0.25-micron process. Because logical TMDS-interface processing does not carry the I/O-transistor limitations of its electrical signaling, you can seamlessly integrate it onto a processor without adversely affecting the choice of process technology or cost.

For this reason, graphics-chip-set designers directly implement HDMI- and DVI-protocol processing and a full DisplayPort interface onto their chips to

Support **Across The Board**™

Bryan Fletcher
Avnet
Global Technical Marketing
Manager

David Loftus
Xilinx
Vice President / General Manager
General Products Division (GPD)

Bringing Products to Life.

At Avnet Electronics Marketing, support across the board is much more than a tagline for us. From design to delivery – we are deeply committed to driving maximum efficiency throughout the product lifecycle.

The Challenge

When the world's largest FPGA maker Xilinx was mounting the launch of its latest Spartan™-3 Generation family of low-cost FPGAs, the company wanted to ensure designers would have everything they need to compete in the highly competitive high-volume market. Xilinx turned to longtime partner Avnet to lend its technical expertise in creating a complete solution.

The Solution

Avnet spent countless engineering hours alongside Xilinx – developing a comprehensive solution of starter kits, development boards, and Speedway™ educational workshops. With Xilinx® Spartan-3 Generation FPGAs and Avnet's support across the board, designers have access to all they need to save up to 50 percent in total system cost over competing FPGAs.

Visit **www.em.avnet.com/xilinxspartan3kits** to learn more about Spartan-3 solutions and to purchase a **Spartan-3A evaluation kit for only $39!**

XILINX®

AVNET® electronics marketing

Accelerating Your Success™

1 800 332 8638
www.em.avnet.com

Avnet Green Initiative

NEDA Supplier Authorized Distributor

facilitate the most efficient bridging. In this architecture, you use an internal multiplexer to select the appropriate logical protocol, and a DisplayPort electrical signal transmits it (**Figure 1**). For a native DisplayPort monitor, the graphics-chip set outputs a DisplayPort electrical signal with the DisplayPort logical protocol. To connect to an HDMI or a DVI monitor, the chip set still outputs a DisplayPort electrical signal. However, the signal now encapsulates the appropriate HMDI or DVI protocol, which you convert by using an external bridge. This approach is attractive because it balances signal integrity, complexity, and cost. Engineers could use a full external bridge between the PC and the monitor. This technique increases overall cost and signal latency, however, because it requires additional circuitry to process and convert both the physical and the logical DisplayPort protocol to HMDI or DVI rather than just the electrical signaling. By implementing HDMI- and DVI-protocol processing on the graphics-chip set, engineers can achieve optimal performance with minimal latency at the lowest cost. Additionally, the bridge—actually, a half-bridge—is necessary only when a non-DisplayPort monitor is in use. As a result, you need to make no major architectural changes to system architectures or graphics-chip sets if a market completes the transition to DisplayPort and thus avoids the associated re-engineering delays and costs.

Engineers have several options for how to implement the external DisplayPort-to-HDMI/DVI bridge, each of which has a different impact on signal quality. For example, they can place the bridge directly on the system board, within a docking station, on a cable adapter, or within the monitor itself. Again, implementing full bridging in the graphics-chip set is not feasible because of 45-nm-process-technology limitations.

On-system-board bridging extends the most reliability because it reduces the number of connectors over which the signal must pass. This approach is also passive, meaning that the supported display interface is fixed, and its primary disadvantage is that the system can support only one display interface—HDMI, DVI, or DisplayPort—but not all of them. The alternative is to support multiple interfaces, each with its own port, but this approach introduces substantial complexity and cost to the main system without enough corresponding benefit.

BRIDGES PRESENT AN OPPORTUNITY TO IMPROVE SIGNAL QUALITY THROUGH A VARIETY OF WELL-ESTABLISHED SIGNAL-ENHANCEMENT TECHNIQUES.

Implementing bridging in a cable adapter, on the other hand, provides the most flexibility, enabling systems to connect to both HDMI/DVI-based monitors and DisplayPort-based monitors. Of the four options, bridging within a docking station has the most limitations. Because relatively few laptop-computer users employ docking stations, it is likely more cost-effective for docking-station OEMs to provide a DisplayPort dongle than to integrate internal bridging. Bridging within the monitor itself is unreasonable because a bridged interface is more expensive than a native implementation.

SIGNAL QUALITY AND ESD

Bridges present an opportunity to improve signal quality through a variety of well-established signal-enhancement techniques. When the bridge receives a signal, it can employ equalization to eliminate jitter sources, depending on the distance and number of connectors between the bridge and the video/graphics-chip set. When transmitting the converted signal, the bridge can add pre-emphasis to the signal to anticipate losses on the path to the monitor.

The impact of signal enhancement can be significant. **Figure 2** shows a signal with a completely closed eye. Passing through jitter-elimination circuitry restores the quality of the signal. Because you can adjust signal enhancement to meet your application's characteristics, signal-path distance and number of connectors become less of a concern with an electrical bridge. Rather than minimizing chip-set-to-connector distances, system engineers have more freedom in graphics-chip-set and connector placement, leading to simplified board design and layout.

In addition to maintaining signal quality, it is important for engineers to protect interfaces connecting to the real world from ESD (electrostatic discharge). The HDMI standard, Revision 1.3, for example, requires 8000V protection at the interface connector. Currently, it is uncertain whether designers can cost-effectively implement 8000V ESD protection in a 45-nm-process technology. In any case, it is not feasible to integrate ESD protection onto a graphics-chip set as doing so would leave the chip set vulnerable if the ESD circuit failed, potentially leading to complete PC-system failure. If it is not economically feasible to repair the problem by replacing the damaged IC or processor, you may need to scrap the entire system. For this reason, designers often implement ESD protection as a discrete device, which is more cost-effective to replace in the case of an ESD failure.

Each passive component in the signal chain, however, not only adds to system cost, but also introduces unwanted capacitance and distortion to any signals it passes through. By integrating ESD protection and bridging circuitry, you can minimize the number of ICs in the signal path. ESD circuitry is also a well-established technology at the 0.25-micron-process technology, which HDMI and DVI bridges currently use. Although such an integrated bridge absorbs the cost of the ESD-protection circuitry better than a discrete approach does, the primary advantage is improved signal quality. A discrete ESD device would interfere with any signal pre-emphasis that the signal source adds. A combined bridge/ESD device, however, not only allows you to implement the pre-emphasis circuitry before the ESD circuitry, but also eliminates the circuit losses and jitter a discrete implementation would introduce. If ESD-protection circuitry fails, it causes only the interface bridge—not the entire system—to fail. Additionally, when your design no longer requires bridging circuitry, you can replace the integrated bridge with a stand-alone ESD device, lowering system cost.

MORE AT EDN.COM

Go to www.edn.com/ms4294 and click on Feedback Loop to post a comment on this article.

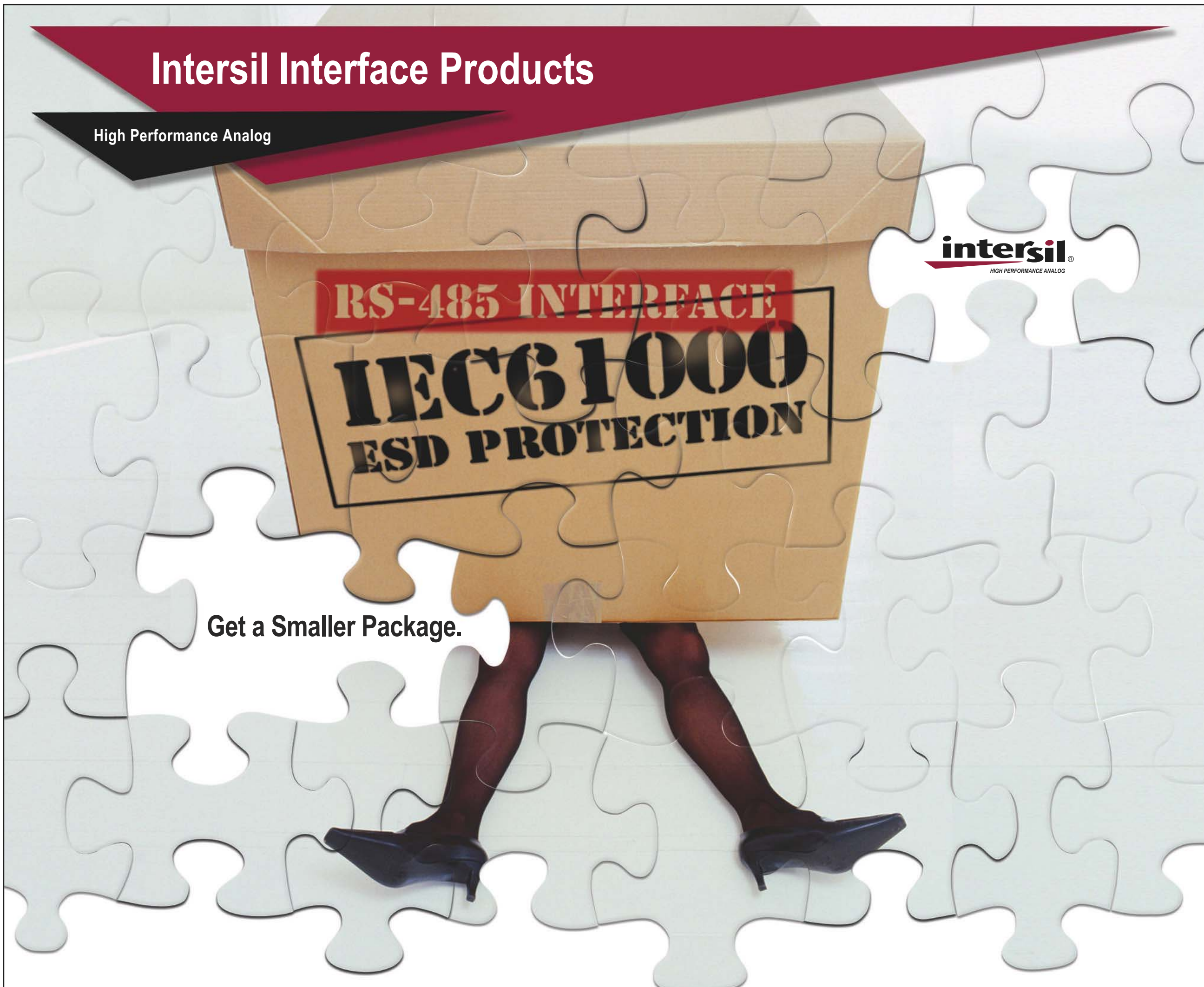
Although it is uncertain whether DisplayPort has what it takes to dislodge HDMI or DVI, DisplayPort is working its way into the PC market. Its extensibility to support new applications and internal chip-to-chip-communication capabilities should extend its reach into other applications that can benefit from its technological and cost optimizations. These applications include digital TV and media gateways aggregating multiple video sources, such as DVD players and computers, over home networks to projection and flat-panel displays.

Today, DisplayPort has wide industry support, including from companies such as Analogix, Dell, Genesis Microchip, Hewlett-Packard, Hosiden Corp, Lenovo, Luxtera, Molex, Parade Technologies, Pericom, Philips, Quantum Data, Samsung, and Tyco Electronics. This year's Consumer Electronics Show saw numerous demonstrations of PC and consumer-electronics equipment, and retailers are selling DisplayPort-enabled monitors.

For the foreseeable future, DisplayPort, HDMI, and DVI will need to coexist. This coexistence will be either a temporary measure as one displaces the others or a permanent move as the industry expands to encompass them all. By understanding the underlying technologies and limitations behind each interface standard, engineers can implement efficient bridging to bring their customers the most flexibility and value at the lowest cost. EDN

AUTHOR'S BIOGRAPHY

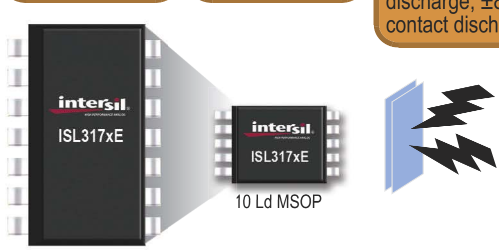
Abdullah Raouf is a product-marketing manager at Pericom, where he has worked for more than three years. In his current position, he manages a $35 million product line, which was only $18 million when he started. Raouf has a bachelor's degree in electrical engineering from the University of California—Davis. His personal interests include "anything competitive—from playing basketball to pushing weight at the gym to closing more design wins than the competition." You can reach him at araouf@pericom.com.



Intersil's new **Full-Featured IEC61000 ESD-Protected 3.3V RS-485/RS-422 Transceivers** save up to 70% of board space.

Along with ±15kV ESD protection, the ISL317xE line of transceivers feature full fail-safe performance against bus faults and hot plug capability to stop data corruption during power-up on an active bus.

- 3.3V eliminates 5V power supply.
- Saves 70% board space over SOIC.
- IEC61000-4-2: ±15kV Airgap discharge, ±8kV contact discharge.



Go to **www.intersil.com** for samples, datasheets and support

ISL317xE Key Features:

- Full fail-safe for predictable performance when bus faults occur.
- Hot Plug capability prevents data corruption during power-up on an active bus.
- Fractional unit load (allows up to 256 devices on the bus).

Device	Data Rate (Mbps)	Slew Rate Limited	Tx/Rx Enable	Package
ISL3170E	0.25	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3171E	0.25	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3172E	0.25	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3173E	0.5	Yes	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3174E	0.5	Yes	No	8 Ld MSOP, 8 Ld SOIC
ISL3175E	0.5	Yes	Yes	8 Ld MSOP, 8 Ld SOIC
ISL3176E	20	No	Yes	10 Ld MSOP, 14 Ld SOIC
ISL3177E	20	No	No	8 Ld MSOP, 8 Ld SOIC
ISL3178E	20	No	Yes	8 Ld MSOP, 8 Ld SOIC

Intersil – Amplify your performance with advanced signal processing.

intersil® HIGH PERFORMANCE ANALOG

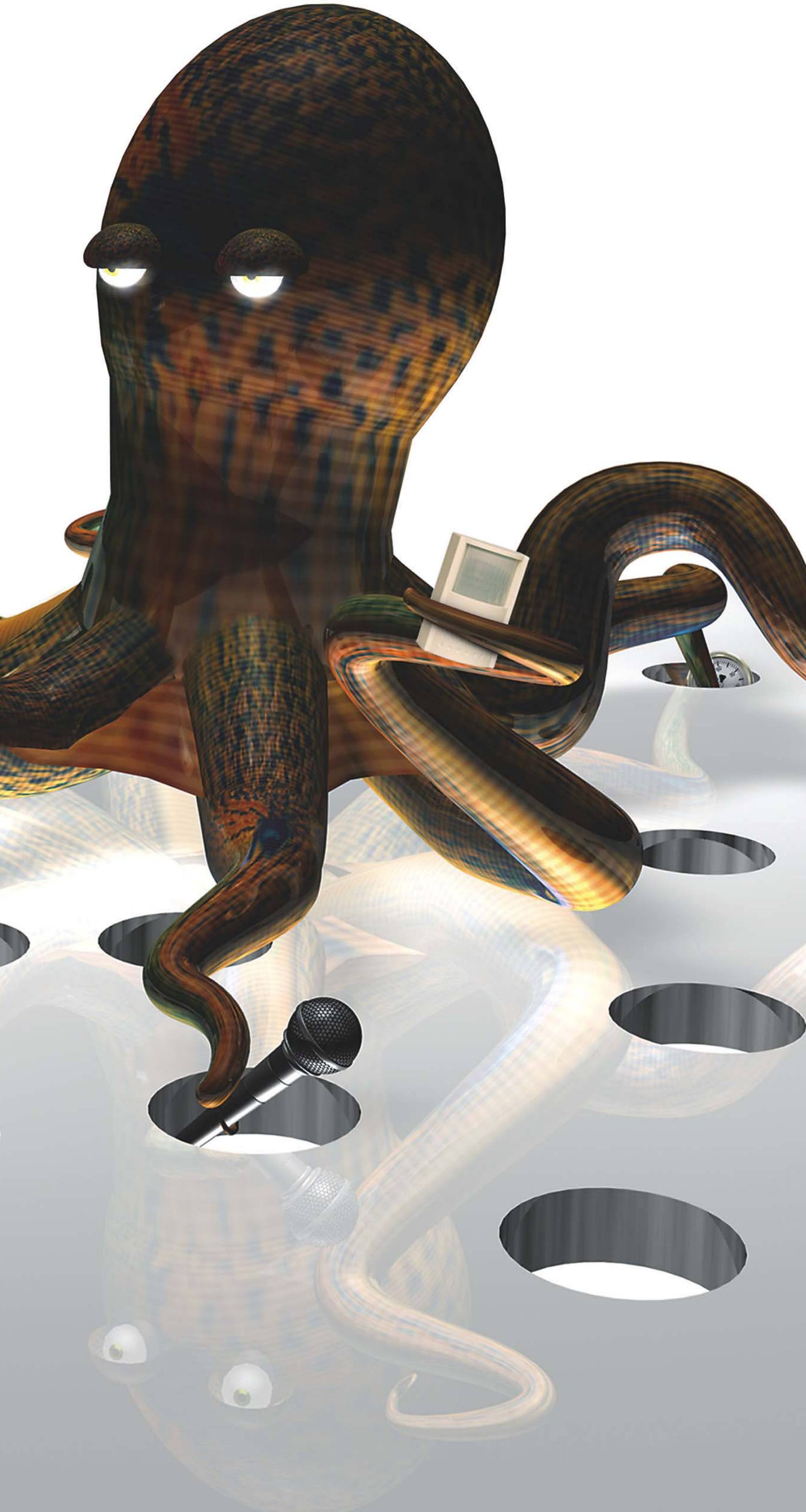
BY ROBERT CRAVOTTA • TECHNICAL EDITOR

Sensor-rich designs

DESIGNERS ARE ADDING SENSORS AND INTELLIGENT PROCESSING TO FILL THE HOLES IN THEIR END-SYSTEM CAPABILITIES, AND IT IS YIELDING DESIGNS THAT COST LESS TO PRODUCE AND OPERATE.

As the cost of microprocessors and sensors continues to drop, autonomous and semiautonomous systems can incorporate more intelligence and make more optimal decisions based on a better understanding of their internal condition and the immediate environment surrounding them. Adding sensors and the intelligent processing to correlate the data from all those sensors to a design incurs a higher design-time cost and complexity, but design teams are increasingly accepting this cost because the trade-off can be a differentiated system that more efficiently delivers more capabilities for prices similar to those of previous designs.

Using sensors in embedded designs is not new. What is changing, though, is that designs are incorporating increasingly more sensors and processors—from high-end autonomous systems to mass-produced consumer appliances. The threshold for replacing mechanical-control structures keeps shifting as sensors and processors continue to drop in price. How companies are partitioning processing and correlating multiple sensors in the same system is going far beyond just mechanical replacement—so much so that vendors often consider their approach as proprietary information because choosing the right mix of sensors and processing algorithms can enable a lower-cost bill of materials, better energy efficiency, and better system performance.



Events such as the DARPA (Defense Advanced Research Projects Agency) Urban Challenge and Grand Challenge demonstrate extremes of how much sensor-rich, fully autonomous vehicles can sense, interpret, predict, interact with, and move within their environment (**Reference 1**). The challenges showcase autonomous automobiles that can drive and navigate entirely on their own without a remote control or human driver by relying solely on various onboard sensors and positioning systems (**Reference 2**). However, in these challenges, their handlers fed the autonomous vehicles a list of goal GPS (global-positioning-system) positions to which they could navigate. They did not decide where to go or in what order to visit the points; rather, they worked out how they should get to each point on the list from their current position.

The DARPA Urban Challenge, which took place on Nov 3, 2007, required autonomous vehicles to drive in urban-road-traffic conditions with other manned and unmanned vehicles while demonstrating that they could safely perform complex maneuvers, such as merging, passing, parking, and negotiating intersections. Six teams successfully completed the DARPA Urban Challenge trial. The winning vehicle, from the Tartan Racing team, employed seven lidar (light-detection-and-ranging), radar (radio-detection-and-ranging), and vision sensors in addition to the inertial GPS/IMU (inertial-measurement-unit) sensor (**Reference 3**). The choice of sensors supported fusion of the data for the planning algorithm and provided some overlap between the sensors for redundancy and correlation of the data.

Robots constitute a growing category of sensor-rich autonomous systems. For example, Boston Dynamics features a number of robots, such as the remote-controlled BigDog, that can navigate and recover while traversing difficult terrains, including icy patches, based on their sensors and onboard-control systems. BigDog's sensors for locomotion include joint position, joint force, ground contact, ground load, a laser gyroscope, and a stereovision system. Additional sensors that focus on the internal health of the system monitor the hydraulic pressure, oil temperature, engine temperature, rotations per minute, and battery charge. Vendor iRobot also produces many types of robots, including consumer-level vacuums, such as the Roomba. The Roomba uses multiple IR (infrared) sensors either directly or with mechanical paddles to sense its environment (**Reference 4**).

Semiautonomous systems are a growing area for sensor-rich designs. On the high end are fly-by-wire aircraft and automobiles, and on the low end substantial growth is occurring in consumer appliances, such as washing machines. A semiautonomous system accepts some high-level direction from a human operator but is responsible for managing the low-level operational details of the system it monitors and controls. With a broad enough interpretation, most embedded systems fall into this category, and the designers of these systems may benefit from the lessons they learn from other sensor- or data-rich designs (see **sidebar** "Supercomputing").

Complex remote-controlled systems, such as BigDog, must autonomously respond to their immediate environment and condition, partially because a remote-control interface is insufficient from a data-bandwidth and feedback-interface perspective for an operator to order the myriad adjustments for the system to behave properly. When a design team chooses to implement a semiautonomous subsystem, it should perform its task as well as, faster than, or better than most operators could manually perform that same task.

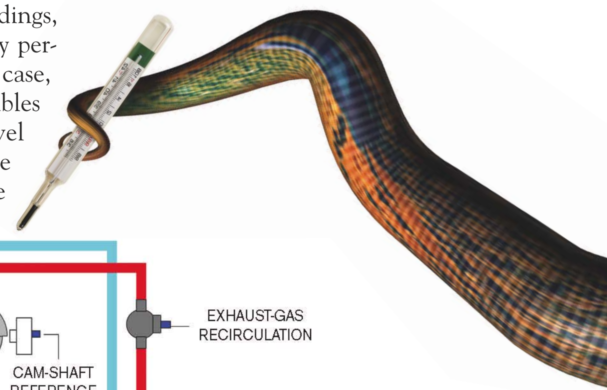
AT A GLANCE

- Correlated-sensor processing is a leading-edge and increasingly sophisticated technology.
- Sensors are becoming smarter as designers place more processing capabilities into them.
- All types of applications—from high-end to low-end systems—are benefiting from using a richer set of sensors to enable them to handle more complex usage scenarios.

The semiautonomous fly-by-wire flight-control system for aircraft replaces the physical control between the pilot and the aircraft with an electrical interface. The control system receives the pilot's commands and then determines how best to exercise the actuators, based on its own sensor readings, at each control point to optimally perform the desired behavior. In this case, the smarter control system enables the pilot to focus on the high-level control of the aircraft while the flight-control system manages the low-level control of each of the subsystems; this approach frees up valuable cognitive cycles for the pilot to focus on those environmental issues for which the flight-control system cannot compensate.

Automobiles are increasingly employing this same split in high- and low-level control between the driver and the onboard-control subsystems to make them safer and more efficient (**Reference 5**). Examples of autonomous subsystems within automobiles include antilock-braking systems; electronic-stability control; traction control; yaw control; and collision-mitigation systems, such as intelligent restraint systems and air bags. Depending on the circumstances, the driver may be unaware of these control systems.

The automotive-engine-management system represents a sensor-rich, semiau-



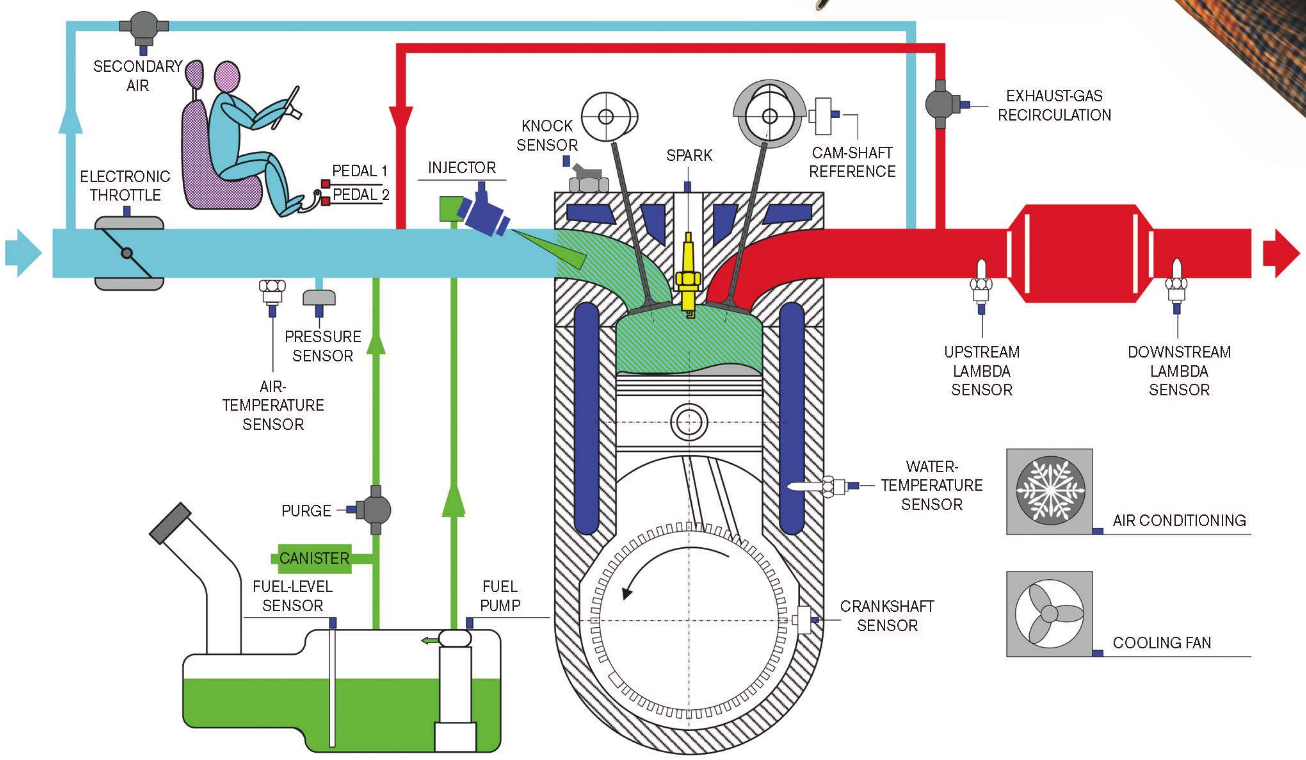


Figure 1 An automotive-engine-management system can correlate more than a dozen sensors to optimize engine operation (courtesy Infineon).

Ultra-Low Power LDOs

150mA, 500nA I_Q Regulators for MCU-Based Applications

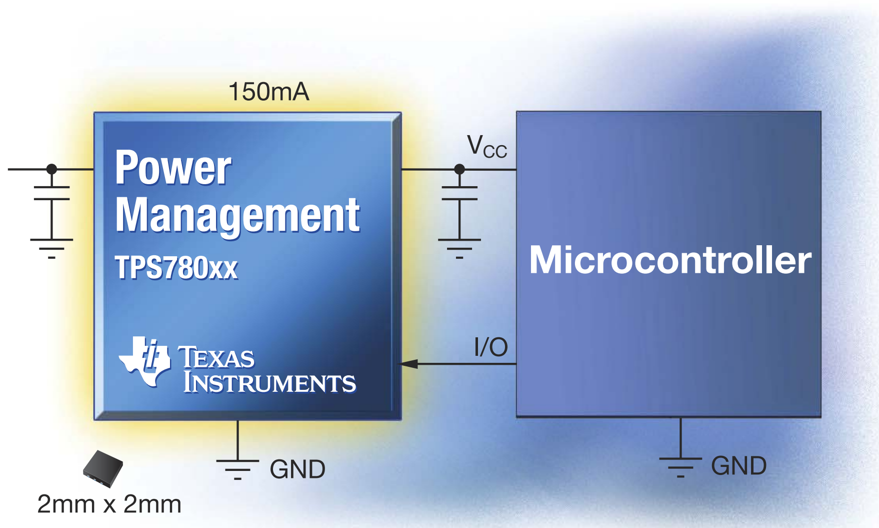
High-Performance Analog>>Your Way™

Applications

- TI MSP430-based applications and other microcontrollers
- Power rails with programming mode
- Wireless handsets and other low-power, battery-powered products

Features

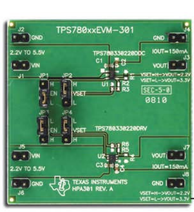
- Low I_Q: 500nA (typ)
- Available in fixed output voltages from 1.5V to 4.2V using innovative factory EPROM programming
- Available in adjustable versions from 1.22V to 5.25V
- V_{SET} pin toggles output voltage between two factory-programmed voltage levels
- Stable with a 1.0µF ceramic capacitor
- Logic level compatible enable pin
- Price: $0.65 (1k)



TI's **TPS780xx** LDOs with dual-level voltage output for low-power, battery-powered devices consume only 500nA of quiescent current. The LDOs implement dynamic voltage scaling (DVS), using a voltage select (V_{SET}) pin to allow switching between two voltage levels to customize and cut power consumption.

Device	V_{IN} (V)	I_{OUT} (mA)	V_{OUT} (V)	I_Q (µA)	Package	Price (1k)*
TPS780xx	2.2 - 5.5	150	1.22 - 5.25	500nA	TSOT-23, SON	$0.65
TPS781xx	2.2 - 5.5	150	1.22 - 5.25	1	TSOT-23, SON	$0.50
TPS797xx	1.8 - 5.5	10	1.25 - 4.9	1.2	SC70	$0.34
TPS715xx	2.5 - 24	50	1.2 - 15	3.2	SC70	$0.34
TPS715Axx	2.5 - 24	80	1.2 - 15	3.2	SON	$0.44

** Suggested resale price in U.S. dollars in quantities of 1,000.*



www.ti.com/tps780xx 1.800.477.8924 ext. 4490

Get Evaluation Modules, Samples and Power Management Selection Guide

Texas Instruments

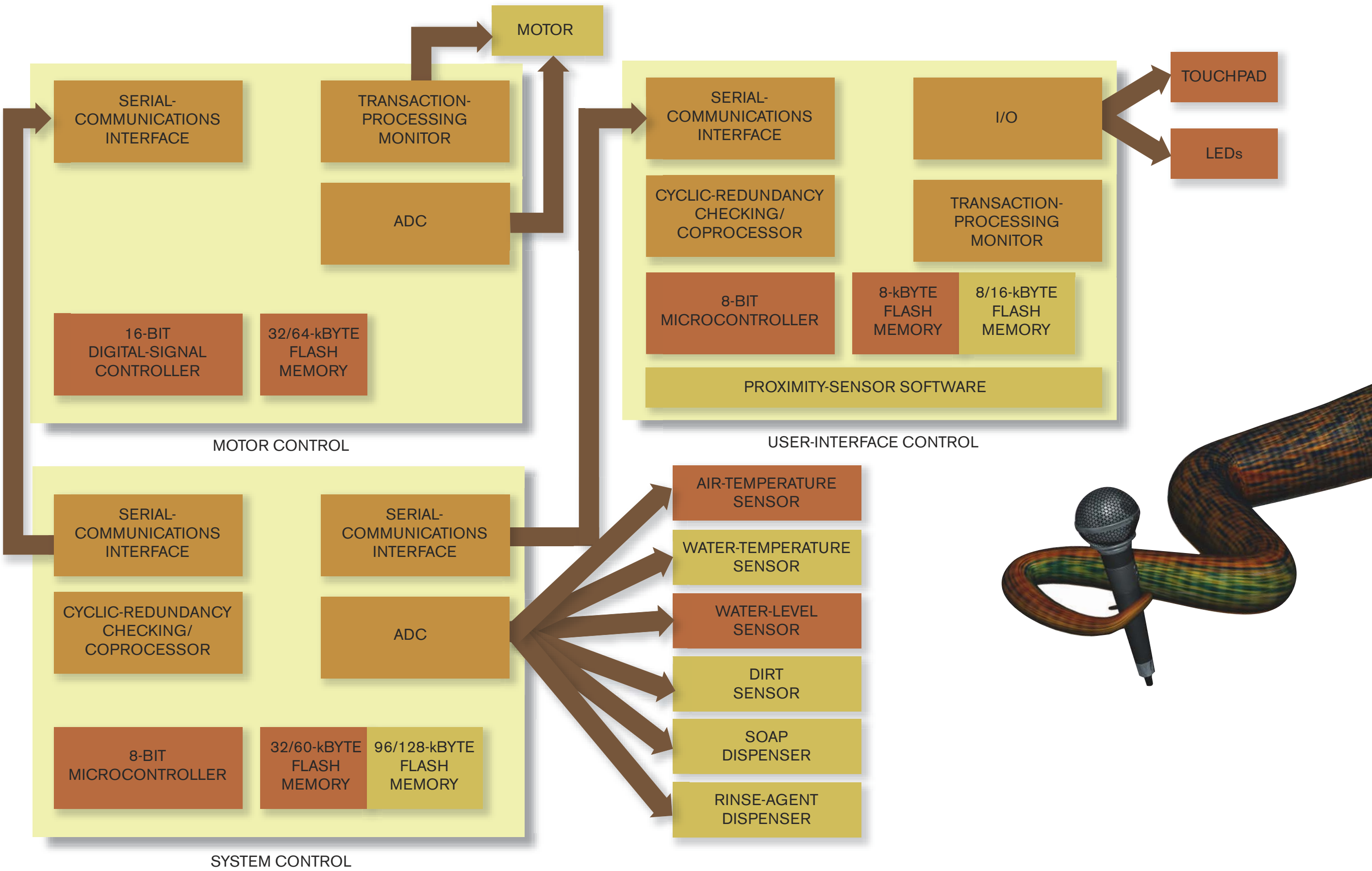


Figure 2 Using multiple sensors to make decisions requires extra memory for each sensor to support buffering and the processing for correlating the data with other sensor inputs (courtesy Freescale).

tonomous embedded subsystem (**Figure 1**). In addition to monitoring the pedal interface with the driver, the system tracks many other internal data points, such as temperature, pressure, and chemical composition of the air, fuel, and exhaust within the system, and performs further correlations with other sensors measuring the spark, knock, and crankshaft position to optimize engine-power output, fuel efficiency, emissions performance, and driving experience, or even to accommodate alternative fuels.

FALSE POSITIVES

In addition to the considerations for design and implementation costs, a semiautonomous embedded-control system's ability to resolve ambiguous and undefined conditions limits the scope of such systems. An "enhanced" system greatly diminishes in value if it requires too much operator intervention because it issues too many false warnings or because it might damage the end system. The decrease in reliability for the electronic systems in Mercedes automobiles in the early 2000s exemplifies how a system's inadequate resolution of ambiguous or undefined conditions can negatively impact the value of the whole system.

In this case, correlating more sensor data is enabling semiautonomous embedded-control systems to safely take on more complex decisions because they are increasingly able to adequately identify and avoid acting on false-positive conclusions. Collision detection on a high-end automobile can rely on many sensors operating in concert, such as long- and short-range radar, IR, video, inertial, and ultrasonic sensors, to detect and validate the necessary actions to a potential or imminent collision. Each of these sensors provides information about the surrounding environment that the control system can partially correlate with the data from the other sensors to fill in the blind spots of each type of sensor to avoid undesirable decisions—such as deploying an air bag when a pebble hits the bumper of the vehicle.

A growing class of warning subsystems in automobiles that provide warning assistance, such as for lane-departure and blind-spot detection, interacts directly with the driver to provide information or assistance. These warning and response systems rely on correlating multiple sensor inputs to avoid issuing false alarms or responding incorrectly to a condition. For example, a lane-departure-detection subsystem could correlate data among visual, inertial, wheel-position, and steering-column-position sensors before issuing a warning to the driver so as to avoid issuing false alarms.

As vendors resolve the cost and design-complexity issues of using more sensors and processing intelligence in embedded-control systems, designers are incorporating more sophisticated autonomous-control systems in lower-cost designs, including midrange consumer applications. Priyabrata Sinha, principal applications engineer at Microchip, points out that appliances are stepping outside the state-machine box and add-

ing more sensors and intelligence into the decision loop.

For example, contemporary washing machines can use three microcontrollers to manage the system and the user interface (**Figure 2**). An interesting thing to note is that the amount of flash memory—not the processor architecture's size—is the most significant difference between the example two- and six-sensor designs. The extra memory allows the system to incorporate additional code for the new sensors and allows the program code to correlate the inputs that the more complex control algorithm uses.

A key area of opportunity for "fast"-response systems is how designers pair and connect sensor processors, says Ritesh Tyagi, senior product/segment manager at Renesas Technology America. A midrange-priced refrigerator may use as many as eight microcontrollers with the appropriate set of localized sensors to provide custom and optimal control for each of the refrigerator stations, such as the meat and vegetable drawers. These types of implementations are striking a

MORE AT EDN.COM

For related blog posts about embedded processing, go to www.edn.com/blog/1890000189.html.

For a related article about sensor fusion in smarter automobiles, go to www.edn.com/article/CA6339246.

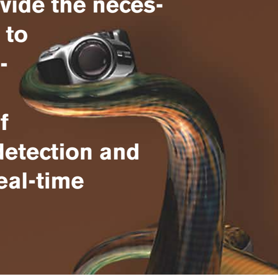
Go to www.edn.com/080710cs and click on Feedback Loop to post a comment on this article.

SUPERCOMPUTING

Sensor fusion involves combining sensory data or data you derive from sensory inputs that results in information that is, in some sense, more accurate, more complete, or more dependable than would be possible when you use these sources individually. In some cases, the data may come from a single type of sensor that collects a tremendous amount of similar data about some topic, such as a CT (computed-tomography) scan, an MRI (magnetic-resonance-imaging) scan, financial-market figures, drug and genetic matching, or even the tremor data from an impulse signal into the ground that will ultimately uncover hidden oil deposits. So much data exists in these types of scenarios that it is impossible for a human to make complete sense of it until a computer has preprocessed it into a manageable and usable format. The amount of data that is available for correlation is so significant that producing usable information in a reasonable amount of time requires supercomputer structures involving many processors.

Radiologists benefit from CAD (computer-aided-detection) technology that applies supercomputing and large amounts of data correlation to provide what amounts to a second pair of eyes to assist them in reading and interpreting medical images. The CAD software does not replace the imaging technology; rather, the computationally intensive process can provide visualization assistance when interpreting medical images. One of the tradeoffs in CAD-based systems such as this one is the quality of the data correlation and the time it takes to arrive at that level of quality. When the CAD software identifies features in a medical image, it brings them to the attention of the radiologist as a means of decreasing the number of false-negative readings. The medical sector uses CAD in a production capacity in CT exams, mammography screenings, and solid-lung-nodule examinations with equipment such as the ImageChecker system from Hologic.

The lessons users learn from systems such as these supercomputing applications may provide the necessary insight into how to enable future embedded-control systems to become capable of even more complex detection and decision-making in real-time scenarios.



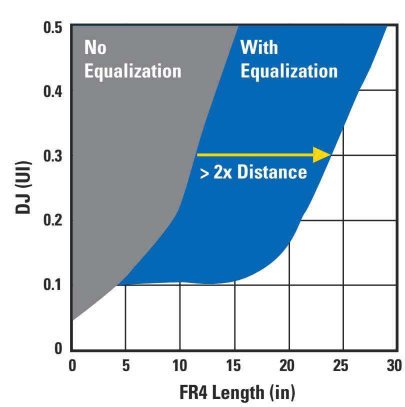
POWERWISE®

Decrease Heat

National's PowerWise® solutions provide optimal performance at the lowest power

Find nearly 300 PowerWise products that are top performers in efficiency based on competitive metrics across 24 categories, including:

- **Power-Saver equalizers** more than double signal distance at up to 12.5 Gbps while consuming zero power
- **Synchronous switching regulators** are ≥95% efficiency for point-of-load conversion applications
- **High-voltage PWM controllers** convert input voltages up to 100V at ≥85% peak efficiency
- **High-precision temperature sensors** feature TruTherm® technology for >0.75°C accuracy with greater thermal and fan speed control



DS80EP100 12.5 Gbps Power-Saver Equalizer performance graph

Find PowerWise products, metrics, white papers, app notes and tools at:

national.com/powerwise

National Semiconductor

balance between centralized and distributed processing to provide better reliability, meet an aggressive power budget, and simplify the user interaction with the appliance.

Unfortunately, the approach of using multiple types of sensory data and correlating them together in the control algorithms is a sensitive proprietary topic for many companies. However, the few high-level examples here might provide you with the inspiration to explore whether additional ways exist for you to collect sensory information and correlate it with the other information in the system to make a better design that can more efficiently perform new value-added functions at lower overall cost. **EDN**

REFERENCES

1 "DARPA Urban Challenge," www.darpa.mil/grandchallenge.

2 Cravotta, Robert, "Operating alone," *EDN*, Dec 5, 2005, pg 49, www.edn.com/article/CA6288032.

3 "Tartan Racing: A Multi-Modal Approach to the DARPA Urban Challenge," April 13, 2007, www.darpa.mil/grandchallenge/TechPapers/Tartan_Racing.pdf

4 Cravotta, Robert, "Rummage through a Roomba," *EDN*, March 15, 2007, pg 32, www.edn.com/article/CA6421379.

5 Cravotta, Robert, "Making vehicles safer by making them smarter," *EDN*, June 8, 2006, pg 49, www.edn.com/article/CA6339246.

FOR MORE INFORMATION

Altera
www.altera.com

Acceleware
www.acceleware.com

Boston Dynamics
www.bostondynamics.com

Freescale
www.freescale.com

Hologic
www.hologic.com

Infineon
www.infineon.com

iRobot
www.irobot.com

Microchip
www.microchip.com

Renesas
www.renesas.com

Texas Instruments
www.ti.com

UAV Forum
www.uavforum.com

Xilinx
www.xilinx.com

You can reach Technical Editor Robert Cravotta at 1-661-296-5096 and rcravotta@edn.com.

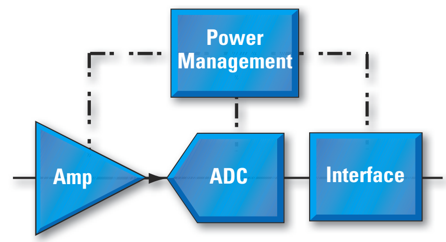
PowerWise®

Optimize Performance at the Lowest Power

National's PowerWise® Solutions Help Engineers Design Energy Efficient Systems

PowerWise products are analog and mixed-signal semiconductors that balance higher performance with lower power consumption.

PowerWise subsystems are architectural innovations designed to enable energy-efficient systems.



PowerWise Metrics Help Designers Compare Analog Components

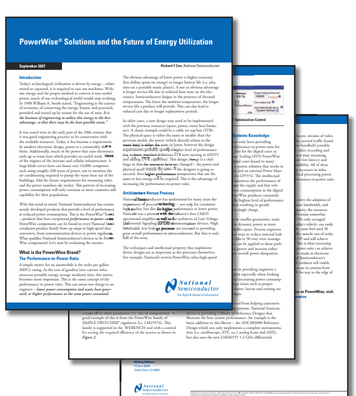
PowerWise metrics are formulas and thresholds that distinguish energy efficient components from those that are less efficient. National has developed PowerWise metrics for 24 product categories and selected the best-in-class energy efficient products in each of these categories. Each PowerWise product has a PowerWise label and rating which summarizes its key specifications.

PowerWise® Efficiency Ratings
(4 out of 24 categories shown)

Product Family	Metric	Threshold	Units
Switching Regulators	Peak Efficiency	≥ 95	%
High-Speed ADCs	$\frac{P}{2^{ENOB} \cdot F_s \cdot ch}$	≤ 2.5	pJ/conversion
Equalizers	$\frac{P}{T_r \cdot ch}$	≤ 20	pJ/bit
Timing Solutions	$\frac{P \cdot t_j}{ch}$	≤ 55	mW•pS

PowerWise Resources Help Designers Improve System Performance to Power

Visit *national.com/powerwise* for white papers, app notes and design tools that help system engineers by highlighting the optimal balance between performance and power consumption at the component, subsystem and system level.



Find PowerWise products, metrics, white papers, app notes and tools at:

national.com/powerwise

National Semiconductor

TECHNOLOGY *edge*℠

PowerWise® Solutions and the Future of Energy Utilization

White Paper

Richard F. Zarr, Chief Technologist

Introduction

Today's technological civilization is driven by energy – whether stored or captured, it is required to run our machines. Without energy and the proper method to convert it into useful power, much of our technological world would stop working. In 1908 William A. Smith stated, "Engineering is the science of economy, of conserving the energy, kinetic and potential, provided and stored up by nature for the use of man. ***It is the business of engineering to utilize this energy to the best advantage, so that there may be the least possible waste.***"

It was noted even in the early part of the 20th century that it was good engineering practice to be conservative with the available resources. Today, it has become a requirement. In electronic design, power is a finite commodity. Additionally, much of the power that runs electronics ends up as wasted heat which provides no useful work. Think of the engines of the Internet and cellular infrastructure. A large blade server farm can house over 10,000 computers each using roughly 200 watts of power, not to mention the air conditioning required to pump the excess heat out of the buildings. Add the future requirements for streaming video and the power numbers sky rocket.This pattern of increasing power consumption will only continue as more countries add capability for their populations.

With this trend in mind, National Semiconductor has continuously developed products that provide a level of performance at reduced power consumption. This is the PowerWise brand – products that have exceptional performance-to-power ratios. PowerWise components can be found in every National product category from interface products to high-speed data converters, from communication devices to power regulators. What qualifies National's products as PowerWise components? Let's start by evaluating the metrics.

The Performance-to-Power Ratio

A simple metric for an automobile is the miles per gallon (MPG) or kilometer per liter (KPL) rating. As the cost of gasoline (our current infrastructure portable energy storage medium) rises, this metric becomes more important. This is the same concept as the performance-to-power ratio. This can mean two things to an engineer – ***lower power consumption and excess heat generated, or higher performance at the same power consumed.***

The obvious advantage of lower power is higher economy (less dollars spent on energy) or longer battery life (i.e., play time on a portable music player). A not so obvious advantage is longer service life from reduced heat wear on the electronics from semiconductor fatigue in the presence of elevated temperatures. The lower the ambient temperature, the longer service life a product or system will provide. This can also lead to reduced cost due to longer replacement periods.

In other cases, a new design may need to be implemented with the previous resources (space, power, waste heat limits, etc). A classic example could be a cable set-top box (STB). The physical space is either the same or smaller than the previous model, the power (which directly relates to the waste heat) is either the same or lower, however the design requirements probably specify a higher level of performance (i.e., a classic standard definition STB now moving to HDTV and adding DVR capability). This design change is a challenge in that the resources have not changed – the power and physical space remain the same. If the designer is going to succeed, then higher performance components that use the same or less energy will be required. This is the advantage of increasing the performance-to-power ratio.

Architecture Versus Process

National has understood for many years the importance of process technology – not only for consistent high quality, but also for higher performance at lower power. National was a pioneer with the industry's first CMOS operational amplifier as well as the architects of Low Voltage Differential Signaling (LVDS) communication devices and Low Dropout Regulator (LDO). High-bandwidth, low-

PowerWise®

National Semiconductor

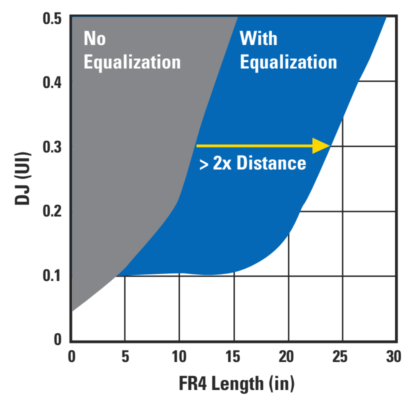
PowerWise®

Decrease Heat

National's PowerWise® Solutions Provide Optimal Performance at the Lowest Power

Find nearly 300 PowerWise products that are top performers in efficiency based on competitive metrics across 24 categories, including:

- **Power-Saver equalizers** more than double signal distance at up to 12.5 Gbps while consuming zero power
- **Synchronous switching regulators** are ≥95% efficiency for point-of-load conversion applications
- **High-voltage PWM controllers** convert input voltages up to 100V at ≥85% peak efficiency
- **High-precision temperature sensors** feature TruTherm® technology for >0.75°C accuracy with greater thermal and fan speed control



DS80EP100 12.5 Gbps Power-Saver Equalizer performance graph

Find PowerWise products, metrics, white papers, app notes and tools at:

national.com/powerwise

National Semiconductor

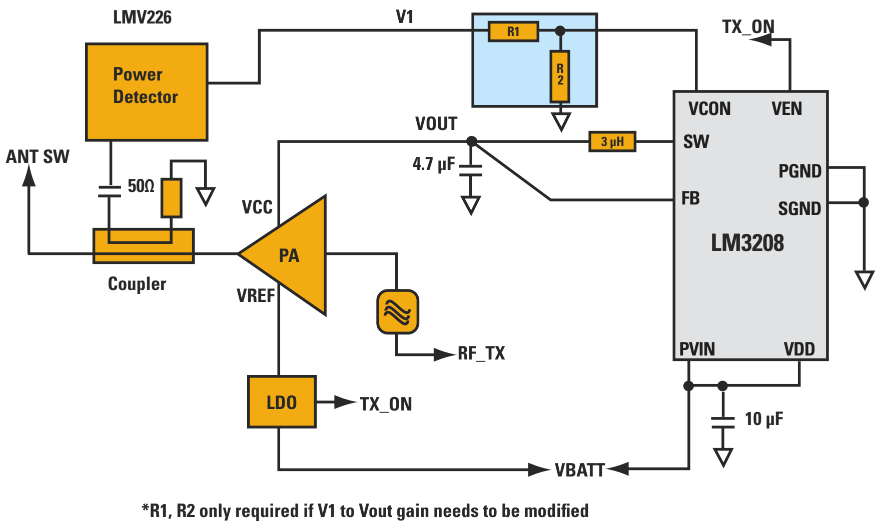


Figure 1. Adaptive RF Power Subsytem

leakage processes are essential to providing great overall performance in semiconductors. But that is only half of the story.

The techniques and intellectual property that implement device designs are as important as the processes themselves. For example, National's newest PowerWise ultra-high-speed Gigasample ADC083000 A/D Converter uses a novel folding converter topology that greatly reduces the power required to sample at 3 Gigasamples per second at less than 2 Watts. This is an architecture that greatly reduces power consumption over other converter architectures such as flash converters. The folding architecture also scales well where flash converters double their power consumption with every bit of resolution that is added.

Systems Versus Components

Another important aspect of the performance-to-power ratio metric is not always apparent in looking at individual components. It is how these components enable lower power consumption. A good example of this is the use of Adaptive RF power in handsets (see ***Figure 1***.) Using the LM3208 in combination with the LMV228 power detector, the Pdc component of the PA can be dramatically reduced – both of these devices would be considered PowerWise products for systematically reducing power in a cellular handset output stage.

Tools for Increasing Efficiency

There is another category that makes a National device part of the PowerWise family, and that is the availability of tools to optimize their implementation. Some components need to have tools to help facilitate a high performance-to-power ratio. This applies mostly but not exclusively to switching power regulators. WEBENCH® design tool allows the engineer to "dial in" a performance level for power supply designs as a trade off to other parameters (i.e. size of components). A good example of this is the fourth generation SIMPLE SWITCHER® family (i.e., LM25576). This family is supported in the WEBENCH tool with a control for optimizing the design of the system with trade-offs between conversion efficiency and footprint as shown in ***Figure 2***.

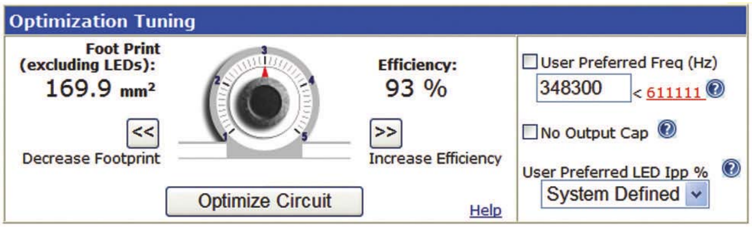


Figure 2. WEBENCH Optimization Control

Intellectual Property and Systems Knowledge

National has not only been providing solutions for increasing the performance-to-power ratio for the analog sections of systems, but for the digital cores as well. National's PowerWise Adaptive Voltage Scaling (AVS) solutions have been used in digital cores found in many cellular handsets. This is truly a system solution that works in combination with the processor and an external Power Management Unit (PMU) such as the LP5552. The intellectual property in the processor core monitors the performance of the system and adaptively adjusts the supply and bias voltages to significantly reduce power consumption in the digital processor up to 70%. AVS PowerWise products constantly adjust in real time to provide the highest level of performance at the lowest power consumption resulting in greatly increased operating time from a single charge.

As digital processes shrink to ever smaller geometries, static power will begin to overtake the dynamic power as more transistors are packed into a smaller space. Process engineers are constantly struggling to find ways to reduce internal leakage which at larger geometries (above 90 nm) were manageable. PowerWise AVS solutions can be applied to these problems to greatly reduce the static power and increase either run time (batteries) or to reduce overall power dissipation.

Reference Designs

Reference designs are important in providing engineers a template for good design practices, especially when looking to increase performance without increasing power consumption. Much of the difficult design issues such as proper component selection and placement, layout and routing are provided in these reference designs.

Building on the knowledge gained from helping customers create high performance analog systems, National is providing a library of reference designs that illustrate the best system performance. An example is the latest addition to this library – the ADC083000 reference design which not only implements a complete instrumentation (i.e., Oscilloscope, Automatic Test Equipment etc.) analog front end (AFE), but also uses the new PowerWise LMH6555 1.2 GHz differential driver as part of the signal chain. This component in combination with our PowerWise ultra-high-speed ADC083000 data converter and timing solutions provides a great starting place for engineers involved in designing instrumentation.

The Future

From Email to Streaming Video

For a good example of why PowerWise energy efficiency is important, let's examine a phenomenon to which most can relate. In the early days, the Internet (circa 1990) was used to move small files and mostly

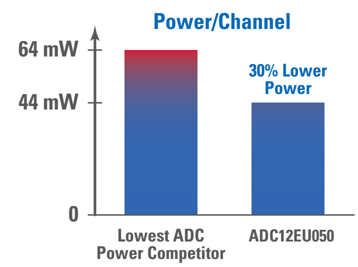
PowerWise®

Increase Reliability

✔ Higher performance
✔ Lower power
✔ Reduced component count

National's PowerWise® Solutions Provide Optimal Performance at the Lowest Power

Find nearly 300 PowerWise products that are top performers in efficiency based on competitive metrics across 24 categories, including:



National's high-speed ADC12EU050 12-bit, CTΣΔ ADC consumes 30% less power than the nearest competitor's product

- **High-speed A/D converters** provide best-in-class performance/power ratios, consuming ≤2.5 pJ/conversion
- **Operational amplifiers** deliver exceptional ≤12 μA/MHz gain bandwidth
- **Timing devices** provide the lowest jitter at the lowest power consumption for maximum data conversion performance
- **Synchronous switching regulators** are ≥95% efficient for point-of-load conversion applications

Find PowerWise products, metrics, white papers, app notes and tools at:

national.com/powerwise

National Semiconductor

emails. Emails of the day only contained text and HTTP was just beginning to be used to support HTML encoded rich content. As the World Wide Web emerged and e-commerce began, the Internet was moving a much larger amount of data traffic including photos and extremely rich content. Once a simple method was found to compress audio (MPEG 1 Layer 3 or MP3), audio was being shipped around as well, absorbing the available bandwidth and driving consumers to find faster connections to the Internet.

Today we see the emergence of a new breed of bandwidth draining content called streaming video. Recent data released by Ellacoya Networks in June, 2007 showed that YouTube accounted for 20% of HTTP traffic or nearly 10% of all Internet traffic. This is the first time that HTTP based traffic has exceeded Pier-to-Pier (P2P) applications such as email. As consumers demand more video over IP networks, it won't only affect the infrastructure, but also the end devices. Mobile video streaming is very demanding and requires not only decompression, but high quality audio. Add in local compression for sending video in real time (now appearing on many handsets), then power is once again being consumed for additional features.

In the not-to-distant future, streams of video with audio will be the normal traffic found on the Internet. Most handheld portable devices will support video recording and playback as well as real-time streaming which will also require low-latency and high-bandwidth availability. All of these features require large increases in infrastructure as well as local processing power. This is why the performance-to-power ratio is so important to design.

Conclusion

As the market forces drive the adoption of streaming video, instant bandwidth, and unlimited storage capacity, the resources required to fuel it all remain finite. According to the US Department of Transportation, in the 1970's automobiles on US highways only averaged 12 MPG, today's vehicles can easily reach 30 MPG on the same fuel used 35 years ago. Additionally, high-performance "muscle cars" of today can easily boast 500 HP and still achieve reasonable mileage. This is what increasing the performance-to-power ratio can achieve. The same gains can be made in electronic devices, and National's PowerWise family of products enable this performance increase in systems from the processor core through the the signal path.

For more information on PowerWise technology, visit:
www.national.com/powerwise

Worldwide Design Centers and Manufacturing Facilities

Design Centers

USA:
Arlington, Texas
Calabasas, California
Chandler, Arizona
Federal Way, Washington
Fort Collins, Colorado
Grass Valley, California
Indianapolis, Indiana
Longmont, Colorado
Norcross, Georgia
Phoenix, Arizona
Rochester, New York
Salem, New Hampshire
San Diego, California
Santa Clara, California
South Portland, Maine
Tucson, Arizona

EUROPE:
Delft, Netherlands
Fürstenfeldbruck, Germany
Unterhaching, Germany
Greenock, Scotland
Kemi, Finland
Milan, Italy
Oulu, Finland
Tallinn, Estonia

ASIA:
Bangalore, India
Hangzhou, China
(joint with Zhejiang University)
Hong Kong, China
Tokyo, Japan

Manufacturing Facilities

Wafer (Die) Fabrication:
Arlington, Texas
South Portland, Maine
Greenock, Scotland

Chip Test and Assembly:
Melaka, Malaysia
Suzhou, China

World Headquarters
2900 Semiconductor Drive
Santa Clara, CA 95051
USA
+1 408 721 5000
www.national.com

Mailing Address:
PO Box 58090
Santa Clara, CA 95052
support@nsc.com

European Headquarters
Livry-Gargan-Str. 10
82256 Fürstenfeldbruck
Germany
+49 8141 35 0
europe.support@nsc.com

Asia Pacific Headquarters
2501 Miramar Tower
1 Kimberley Road
Tsimshatsui, Kowloon
Hong Kong
+852 2737 1800
ap.support@nsc.com

Japan Headquarters
Beside KIBA
2-17-16
Kiba, Koto-ku
Tokyo, 135-0042, Japan
+81 3 5639 7300
jpn.feedback@nsc.com

National Semiconductor

200017-001

BY ERIC SWEETMAN, PHD • VITESSE SEMICONDUCTOR

Measurement-based simulation simplifies analysis of lossy backplanes and cables

A SYSTEMATIC APPROACH USES DSO-BASED TDR AND TDT MEASUREMENTS TO CONSTRUCT MODELS WHOSE SIMULATED RESPONSE DISPLAYS AN UNCANNY RESEMBLANCE TO THE RESPONSE OF THE REAL HARDWARE.

A challenge that often confronts IC designers and support engineers is creating realistic data-channel models and accurately simulating signal transmission through them. Spice models of connectors, vias, and transmission lines work well at lower data rates, but, as data rates approach and exceed 10 Gbps, these models exhibit longer runtimes and become difficult to match to measurements. Behavioral models such as IBIS (I/O-buffer-information specification) execute faster and are evolving toward accurate modeling of transmission lines and nonmonotonic transitions, such as those that incorporate pre-emphasis. All model-based approaches share the problem of matching simulated behavior with that of physical devices, however.

A simulation based entirely on waveforms captured with a DSO (digital sampling oscilloscope) avoids the difficulty of translating physical devices into electrical models (**Figure 1**). You can combine Fourier transforms of time-domain data with S (scattering) parameters derived from TDT (time-domain-transmission) measurements to model signal transmission through complex passive-interconnect systems. Such methods have helped IC designers to simulate the performance of new output drivers over a library of real datapaths and—based on the system's response—to rapidly demonstrate how various parts will perform in a customer's system.

This work began with customer requests for input- and output-port S parameters for asynchronous crosspoint switches in flip-chip BGA packages. Without access to a four-port VNA (vector-network analyzer), applications engineers tried several approaches.

The simplest in concept was to create a TDR (time-domain-reflectometry) test bench in Synopsys HSpice, a version of Spice popular for its W element for transmission-line simulation, and to adjust a multisegment transmission-line model until the simulated TDR provided a good match for the measured TDR. This approach was tedious and resulted in an S_{11} (S-parameter function) that only crudely matched the part's real input behavior.

Applying TDR more directly led to using the FFT (fast Fourier transform) of TDR data to calculate S_{11}. Normalization and de-embedding of board effects were the primary obstacles, but reading previous *EDN* articles led to the use of the current methods (**references 1** and **2**). The normalization process uses the system's TDR response with the BGA part removed from the test board and the solder pads either short or open. In general, the open-pad approach is easier to use on unpopulated boards.

The method captures TDR records from a populated board and a blank board. An FFT routine converts both to the frequency domain. You divide the populated board's complex S_{11} by the unpopulated board's S_{11}. The result is the S_{11} of the BGA part alone. Although Mathcad (www.mathcad.com) easily performed the initial proof-of-principle analysis, later numerical computations used the Scilab (www.scilab.org)

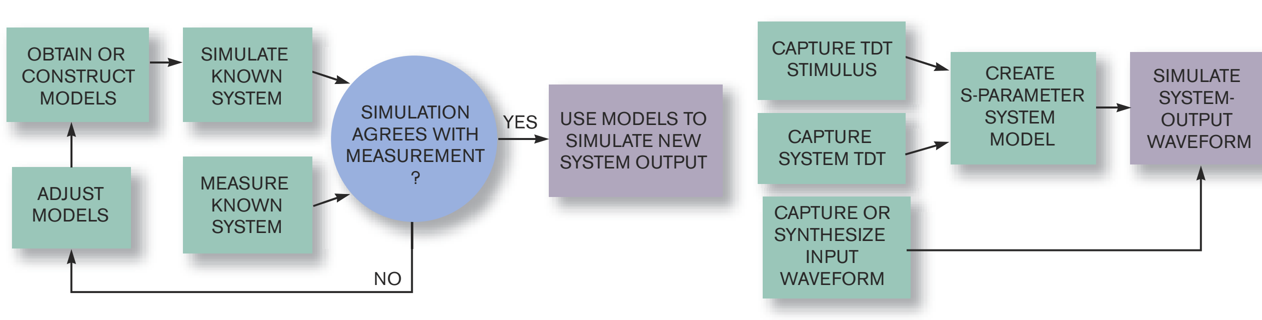


Figure 1 Measurement-based simulation requires acquiring or creating multiple models, such as transceivers, connectors, vias, and striplines. You must adjust the models to match the devices' behavior in a system and then combine them to simulate a new system (a). You can then combine captured or synthesized input waveforms with TDT measurements of the real system to simulate its behavior (b).

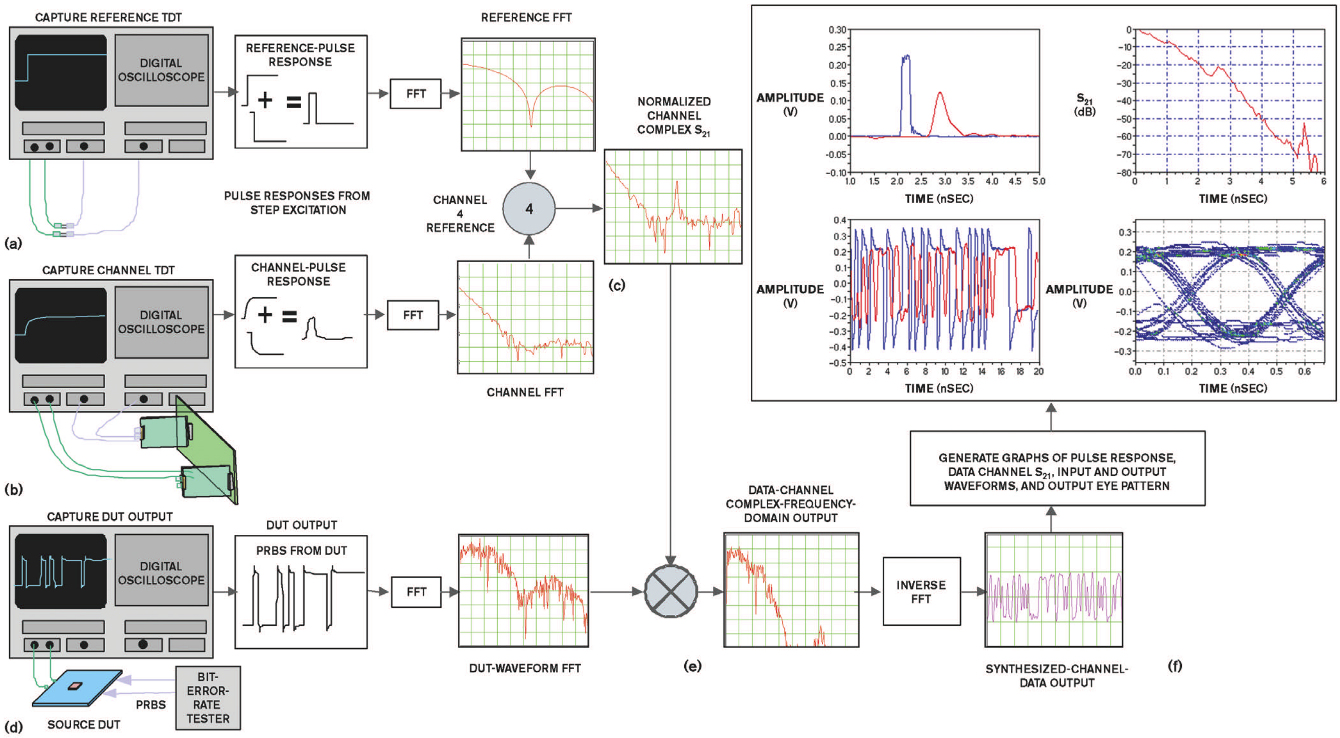


Figure 2 Schematic-data capture and simulation flow follows this path: Start with the TDT-step source (a), the TDT-channel response (b), and a PRBS source (c). Transform the step responses and all waveforms to the frequency domain. Divide these transformed waveforms (d) and multiply them (e) to obtain the system's frequency-domain response. This signal, transformed back to the time domain, appears as a waveform or an eye pattern (f).

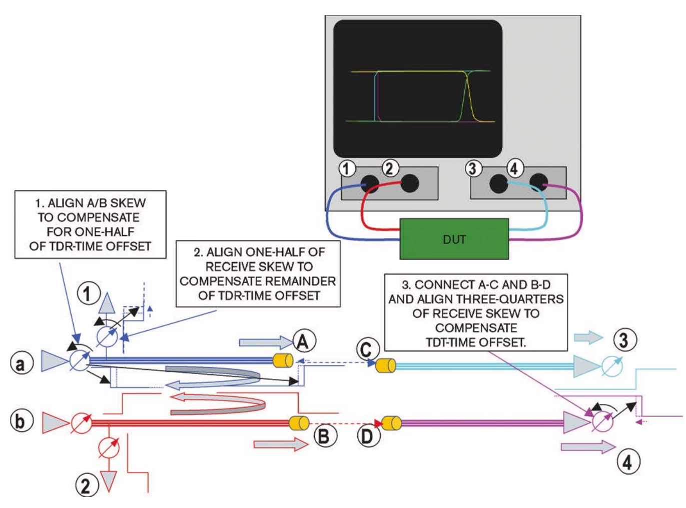


Figure 3 DSO-TDR and -TDT alignment is a three-step process: Observe the TDR signal from open cables. Then, adjust the relative true/complement time to align the signals at cable connectors A and B. Note that this adjustment compensates for only half of the TDR-time mismatch because the observed signals have traversed the cables twice. If you use TDR to generate S_{11} plots, adjust the remaining TDR-time offset at the TDR receivers. After transmission alignment, use short barrel adapters to connect A to B and C to D. Use Channel 4's and Channel 3's skew control to adjust C-3 and D-4.

open-source scientific-software package because of its rich choice of analysis functions.

S parameters can completely describe a linear-data channel. As you can with TDR and S_{11}, you can derive S_{21} from TDT measurements. You can then use these S parameters to model data transmission through backplanes, cables, and other lossy media.

Vitesse (www.vitesse.com) used Scilab to build its simulation environment and based the simulations on TDR and TDT measurements of data channels. This method is flexible because it can capture, simulate, or synthesize stimulus waveforms from step-response waveforms. The simulations transform time-domain data into the frequency domain, in which simple arithmetic operations handle normalization and path effects.

The system stores a library of data channels as TDT-response files along with TDT-normalization measurements it obtains by directly capturing the TDT stimulus. A second library consists of captured or simulated waveforms from different line drivers. These waveforms can be step-function responses or PRBS (pseudorandom-binary-sequence) signals from the same drivers with or without pre-emphasis. **Figure 2** shows a typical simulation sequence. The system captures TDT-waveform data from a lossy backplane's data channel and directly from the TDT-step source and then stores these data in the data-channel library. Both measurements must use the same combination of cables. Both waveforms transform to the complex frequency domain, and their ratio is the data channel's normalized complex-S_{21} response. The channel excitation can be either a captured PRBS waveform or a simulation output from an output-driver model. This time-domain signal trans-

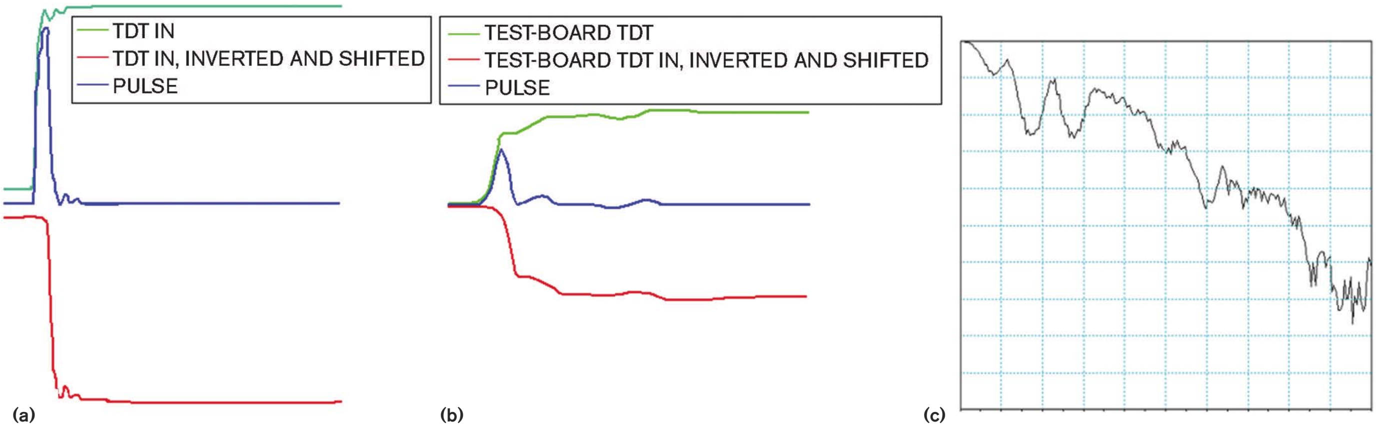


Figure 4 To generate impulse responses and S_{21} from a TDT waveform, start with a reference pulse from the TDT input (a). Next, observe the TDT-output response (b) from the DUT—in this case, an Agilent TDR-test board. Derive the DUT's S_{21} from the input- and output-impulse-response waveforms (c).

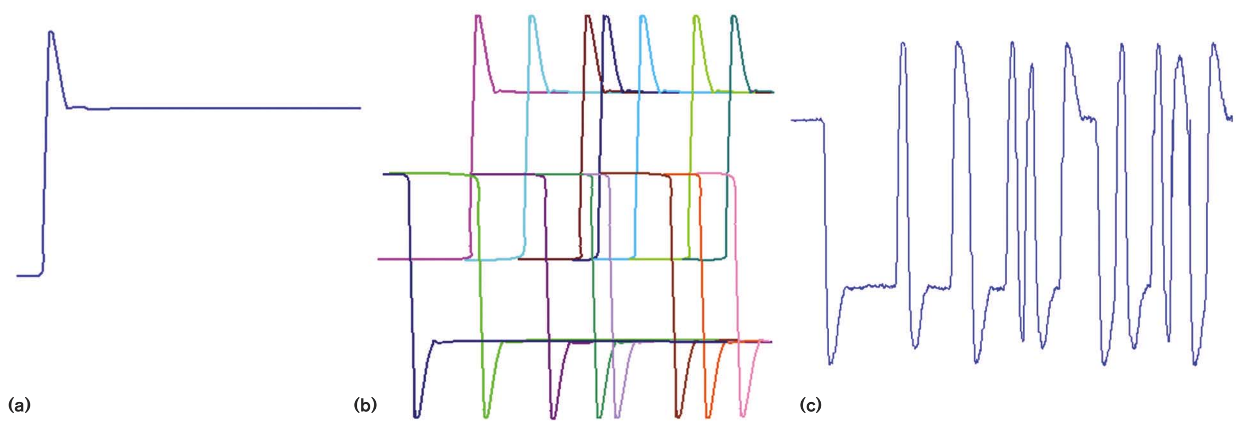


Figure 5 To generate a PRBS from a step response, start with a signal, such as this pre-emphasized step response from a Vitesse asynchronous crosspoint switch (a). Delay multiple copies; add and subtract them to produce a waveform (b). Individual step responses (b) generate the PRBS waveform (c).

forms to the frequency domain, and the normalized channel response multiplies it. Finally, the resulting frequency-domain system response transforms back to the time domain, which displays it as a waveform or an eye pattern.

For TDT-waveform acquisition, you use a DSO with a 35-psec rise-time step source and a 50-GHz-bandwidth input channel. For TDR, the input bandwidth is 20 GHz. A 20-nsec sampling period, 128-waveform averaging, and 4000-point resolution produce good results; averaging for a longer time does little to improve the results.

For differential measurements, you must match the cable pairs as closely as possible and then use the DSO's skew adjustments to better match the step alignment at the DUT's (device under test's) SMA-connector launch point (**Figure 3**). Remembering that the TDR measurement from open cables has double the propagation time of the signal reaching the SMA launch point, set the differential-TDR-step skew adjustment to half the time needed to align the open-cable TDR waveforms. (For TDR acquisition to generate S_{11}, make the remaining half of the skew adjustment on the detector response—in this case, Channel 1 minus Channel 2's skew adjustment.)

Timing alignment is also important for the DSO's receiver channels that capture the TDT waveform. Once you have aligned the launch-cable response, connect the launch cables directly to the receiver cables using SMA barrel adapters and align the TDT-receive-channel skew. Try to achieve 2-psec alignment, but realize that, because the true and complement waveforms are never exactly symmetric, such close alignment can present challenges. In practice, mismatches of 20 psec do not appear to significantly affect the calculated results as long as the imbalance remains constant throughout acquisition of both stimulus and response data.

WAVEFORM CAPTURE

While the launch and receiver cables remain connected, capture a direct-TDT-stimulus waveform, leaving approximately 10% of the time window as a baseline voltage reference before the step (**Figure 4**). You will use this waveform to normalize all subsequent data-channel measurements.

Next, insert the DUT data channel between the input and the output cables and capture a TDT-response waveform, again allowing 10% of the time window for a prestep baseline. Some DSOs don't record timing information. If your instrument doesn't, it is important to keep time-window information for each data file; a simple way is to include the time range in the file name.

Don't try to use an FFT to transform the DSO-captured step-response waveforms directly to the frequency domain. "The worst-possible-case signal to deal with for a DFT (discrete Fourier transform) is the unit-step function" (**Reference 3**). Evaluate the Fourier transform from $-\infty$ to $+\infty$; if the captured data's two endpoints are different, the resulting truncation of a finite time window creates a highly distorted frequency spectrum. The impulse function, which is the derivative of the step function, and the system's TDT response to the step function do not exhibit this problem. Practically, however, the derivative suffers from computational noise. **References 1** and **3** both suggest converting the step response into a finite-pulse response before the DFT. The researcher in **Reference 1** made this transformation by inverting the step response and appending it to the end of the acquired waveform, producing a pulse response whose duration was twice that of the time window. **Reference 3**'s researcher used a pulse excitation, which is the derivative of a step excitation.

A modified version of the approach in **Reference 3** for TDR- or TDT-data delays the waveform by a short time (Δt) and subtracts it from the original signal to create a pulse response with a width of Δt (**Figure 4**). To match the time range of the unshifted signal, the method pads the delayed and subtracted signal at the beginning with the initial level from zero to Δt and truncates at the end by the same amount. The frequency content of the modified data is unchanged, and the value of Δt is not significant. A Δt of less than 90 psec corresponds to the bit width of the fastest Vitesse crosspoint switches, 11 Gbps. The resulting pulse response illustrates the data channel's ISI (intersymbol-interference) effects. This method has the further advantage of creating a 0V baseline, regardless of any measurement offset, such as the one that occurs with ac-coupled signals.

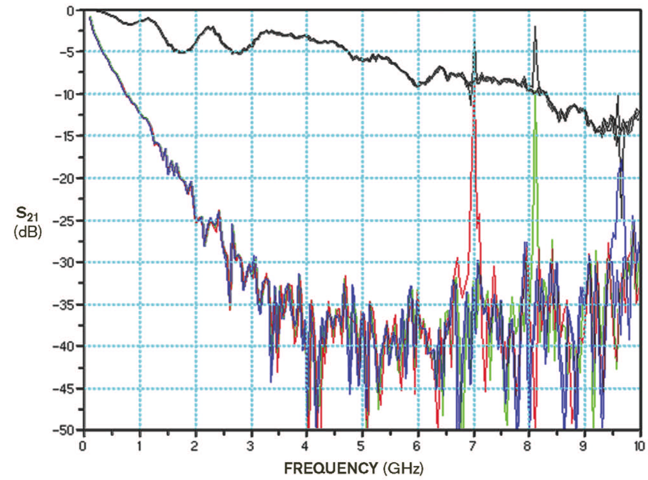


Figure 6 The width of a synthesized pulse affects different data paths differently. These frequency-domain curves are based on TDT data analyzed with three pulse widths of 6.9 GHz at 145, 125, and 105 psec. In the frequency domain, these values result in resonance artifacts. TDT data from 15m of Category 5 cable exhibits these artifacts as peaks at 6.9 GHz (red), 8 GHz (green), and 9.5 GHz (blue), respectively. The upper trace (actually three superimposed traces), from the Agilent TDR-test board, shows artifacts at the same frequencies, but the one at 9.5 GHz is inverted.

With the input and output waveforms converted to pulse functions, calculate S_{21} as the element-wise ratio (Scilab's **./** function) of the complex-pulse-response FFTs to the stimulus FFT. Normalization is automatic. **Figure 4c** plots the magnitude of S_{21} derived from the Agilent (www.agilent.com) test-board's TDT data. In a like manner, you can derive S_{11} from the stimulus and TDR-response FFTs.

OUTPUT-WAVEFORM SIMULATION

Creating reliable S-parameter plots from TDR and TDT data isn't this method's only application. You can also use the method to simulate the effects of a complex path on a data waveform. You can use any waveform as a virtual-signal source, such as the captured PRBS output from a high-speed pattern generator. Because multiplication in the frequency domain is equivalent to convolution in the time domain, you can transform the data waveform into the frequency domain and multiply it, element-wise (**.*** in Scilab) by the datapath's normalized complex S_{21}. The resulting spectrum, when you transform it back into the time domain, is an accurate representation of the source sig-

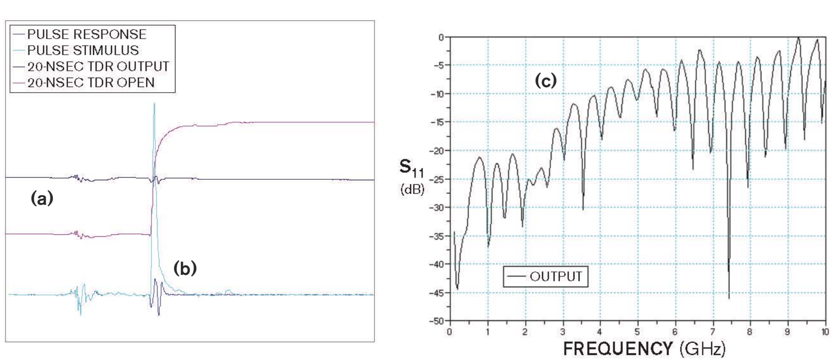
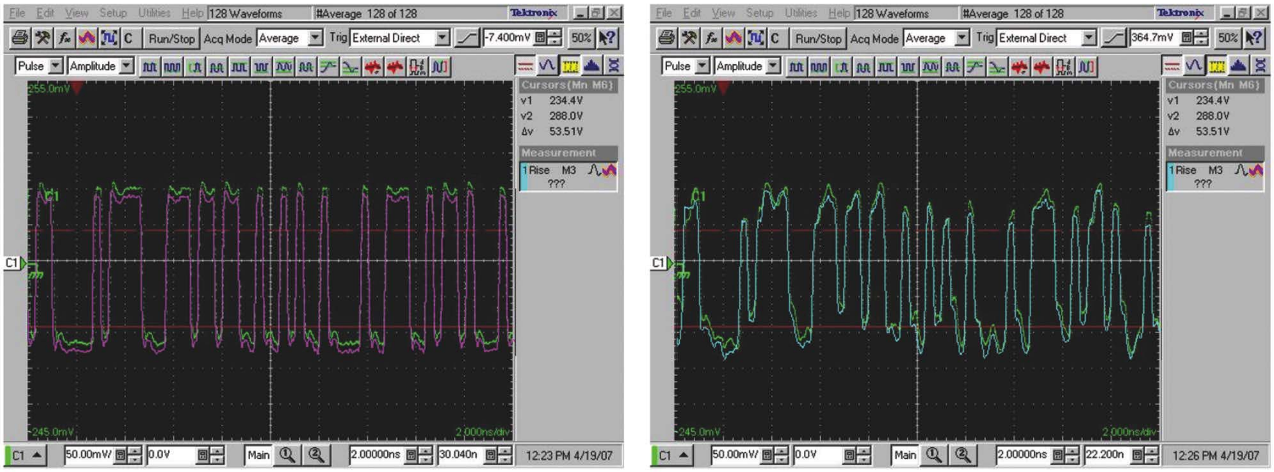


Figure 7 TDR yielded responses at an unpopulated board's output port and at the corresponding port of a populated board of the same design (a); derived impulse and impulse responses (b); and normalized S_{11} with the board effects removed (c).



(a) (b)

Figure 8 Measured test-board results show excellent agreement with simulation: overlay of synthesized (magenta) and measured (green) input waveforms (a) and overlay of simulated (blue) and measured (green) output waveforms (b).

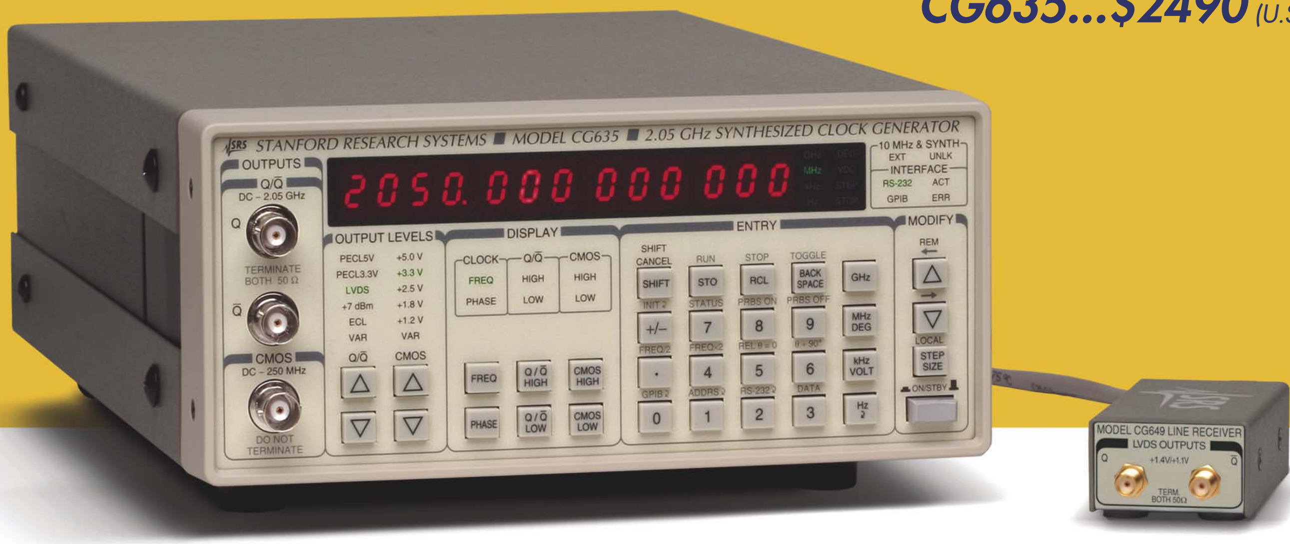
nal propagating through the data channel from which you obtained the TDT.

Vitesse maintains a library of TDT and TDR data from a selection of the backplanes and cables that have passed through the company's laboratory. By using the output from a simulation to stimulate any of the virtual interconnects in its library, the company could, for example, evaluate a new output-preemphasis proposal that engineers had not yet implemented in hardware.

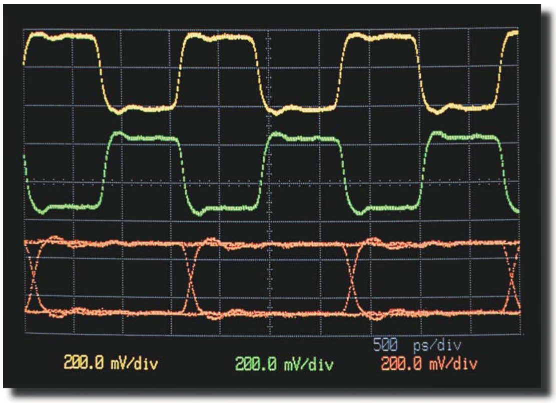
To complement the data-channel library, you might want a library of all likely stimulus waveforms. Unfortunately, though, such a library would be both unnecessarily large and incomplete. A better approach, which works well for Vitesse's asynchronous products, is to use a library of output-driver step

2 GHz Clock Generator

CG635...$2490 *(U.S. list)*



- *Square wave clocks from DC to 2.05 GHz*
- *Random jitter <1 ps (rms)*
- *80 ps rise and fall times*
- *16-digit frequency resolution*
- *CMOS, LVDS, ECL, PECL, RS-485*
- *Phase adjustment & time modulation*



Plot shows complementary clocks and PRBS (opt. 01) outputs at 622.08 Mb/s with LVDS levels. Traces have transition times of 80 ps and jitter less than 1 ps (rms).

The CG635 generates clock signals — flawlessly. The clock signals are fast, clean and accurate, and can be set to standard logic levels.

How fast? Frequency to 2.05 GHz with rise and fall times as short as 80 ps.

How clean? Jitter is less than 1 ps and phase noise is better than –90 dBc/Hz (100 Hz offset) at 622.08 MHz.

How accurate? Using the optional rubidium timebase, aging is better than 0.0005 ppm/year, and temperature stability is better than 0.0001 ppm.

You would expect an instrument this good to be expensive, but it isn't. You no longer have to buy an rf synthesizer to generate clock signals. The CG635 does the job better—at a fraction of the cost.

Stanford Research Systems

Phone: (408) 744-9040 · Fax: (408) 744-9049 · info@thinkSRS.com · **www.thinkSRS.com**

responses to synthesize any arbitrary-waveform pattern. You can use such waveforms as simulation stimuli. The advantage of this approach is that it allows you to create a signal of any rate and pattern from a single library file. You synthesize PRBS waveforms in much the same way as the pulsed waveforms you use to evaluate S parameters from TDT data (**Figure 5**).

Capture a step response from a device at a particular output and pre-emphasis setting along with a hierarchy of step responses for each part in the family and store them in an indexed library for later retrieval. To synthesize a PRBS waveform from the part of interest, repeatedly delay and add or subtract—based on the sign and time delay of each PRBS transition—the step response that corresponds to the desired amplitude and pre-emphasis. Ideally, to facilitate Fourier transformation of the PRBS pattern, you should use an even number of component waveforms so that the synthesized waveform starts and ends at the same level. To simulate data-channel behavior, use this synthesized PRBS pattern just as you would use a captured waveform.

TIPS, CAUTIONS, AND LIMITATIONS

This technique is powerful, but you should observe several precautions when you use it. This method models only differential or single-ended transmission paths. In principle, with additional measurements, you could also model even-mode effects or single-ended, multiport configurations.

The step rise time at the DUT input limits the overall bandwidth. Although the bandwidth relates inversely to the time-domain sampling interval, the frequency-domain resolution is inversely proportional to the time window. With 4000 sample points, the combination of a 20-nsec window and a 5-psec sampling interval appears to represent a good compromise.

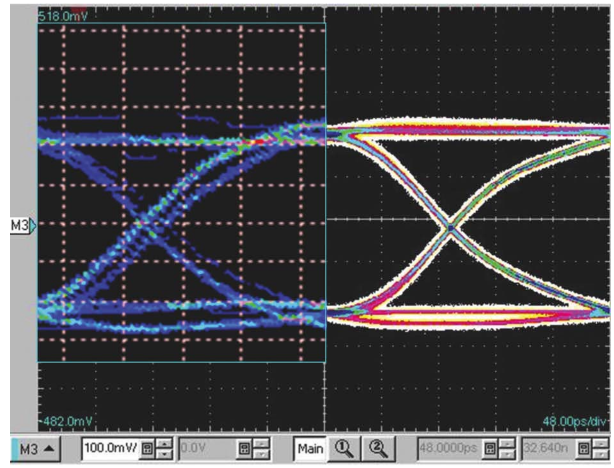


Figure 9 The output of a virtual transmission line (right) driven by a synthesized 4-Gbps PBRS waveform shows excellent agreement with a captured eye (left). These eye plots are for a 2^7-1 PRBS waveform with pre-emphasis from a Vitesse VSC3304HV crosspoint switch driving a 20-in. differential-transmission line.

The source and detector should be proper 50Ω, single-ended, or 100Ω, differential, terminations. The TDT or TDR data accommodates impedance discontinuities within the DUT, but reflections outside the DUT contaminate the simulation.

The DSO's dynamic range limits the S-parameter noise floor. It is important to use a large fraction of the vertical scale, especially for attenuated signals at the far end of a data channel. Averaging helps, but long averaging can lose time resolution to baseline drift. With one model of DSO, a 128-waveform average appears to be a good compromise.

For evaluating differential datapaths, it is important to drive the system with well-aligned true and complement signals. For differential excitation, the true and complement signals should be mirror images, so that you can use either one in place of a differential measurement. However, you must terminate the outputs of both polarities.

Frequency-domain artifacts can occur at the inverse of the synthesized-impulse width (**Figure 6**). The size of these spurs seems, in part, to relate to triggering offsets that, for long transmission paths, are necessary to place the response waveform on-screen. In practice, these artifacts do not significantly alter simulated-response waveforms.

Some examples better demonstrate the features and accuracy of this simulation method. **Figure 7** shows the original application for measurement-based simulation. You capture a differential-TDR waveform from the output port of an evaluation board on which is mounted a BGA-packaged IC. You capture a second TDR from the same port of a second board that contains no BGA device. You process these step-response waveforms to obtain an S_{11} plot with the board effects normalized out.

Figure 8 shows how Vitesse used single-ended TDT measurements in modeling the transmission properties of **Figure 3**'s Agilent TDR-test board. It uses a pre-emphasized step-response-library file of a Vitesse high-speed crosspoint part to synthesize a PRBS waveform. The method combined the TDT-based S_{21} model with the PRBS stimulus to generate an output waveform. A comparison of the synthesized input and output waveforms with real generated and transmitted waveforms shows a remarkable match.

MORE AT EDN.COM

Go to www.edn.com/ms4273 and click on Feedback Loop to post a comment on this article.

The final example compares a synthesized eye plot with captured eye data (**Figure 9**). The stimulus waveform is a 4-Gbps PRBS signal with pre-emphasis from a Vitesse VSC3004HVEV evaluation board; the datapath is a 20-in. differential stripline.

This measurement-based lossy-transmission-path-simulation method has proved useful to the Vitesse Design Center, in which teams routinely use it for such tasks as TDR-based simulation to characterize new parts' input- and output-return loss. Vitesse has used TDT/TDR to measure the frequency dependence of forward and reverse crosstalk and regularly captures a step-response library from new parts to use for virtual testing of customer backplanes. The center maintains a library of lossy media, such as cables and backplanes, which it uses to optimize new part designs. This virtual testbench continues to find new applications. EDN

REFERENCES

1. Pickerd, John J, "Impulse-response testing lets a single test do the work of thousands," *EDN*, April 27, 1995, pg 95, www.edn.com/archives/1995/042795/09df2.htm.
2. Smolyansky, Dima, "Signal-integrity modeling of gigabit backplanes, cables, and connectors using TDR," *EDN*, July 11, 2002, pg 63, www.edn.com/article/CA231568.
3. Andrews, James R, PhD, "Time-domain spectrum analysis and S-parameter vector network analysis," Application Note AN-16, Picosecond Pulse Labs, May 2004, www.picosecond.com.

AUTHOR'S BIOGRAPHY

Eric Sweetman is an applications engineer for Vitesse crosspoint products, providing data sheets and white papers, evaluating schematics, and performing laboratory tests and simulations. He also guides customer engineers in selecting devices and in achieving standards compliance. Sweetman holds a doctorate in physics from the University of Michigan—Ann Arbor and a bachelor's degree in physics from the Massachusetts Institute of Technology (Cambridge). Outside work, he enjoys digital photography and remote-controlled model airplanes.

TAPE-OUT COMES A LOT FASTER
WITH CALIBRE nmDRC.

INTEGRATED SYSTEM DESIGN + DESIGN FOR MANUFACTURING + ELECTRONIC SYSTEM LEVEL DESIGN + FUNCTIONAL VERIFICATION

Calibre® nmDRC | There's nothing like having an advantage when you're racing to market. That's exactly what you get with Calibre nmDRC. Widely recognized as the world's most popular physical verification solution, Calibre's hyperscaling architecture produces the fastest run times available. To accelerate things even more, Calibre nmDRC adds incremental verification and a dynamic results-viewing and debugging environment. Designers can check, fix and re-verify DRC violations in parallel, dramatically reducing total cycle time. Start out and stay ahead of the pack. Go to **mentor.com/go/calibre_nmdrc** or call us at **800.547.3000.**

Mentor Graphics®
THE EDA TECHNOLOGY LEADER

BY SHELLEY GRETLEIN • NATIONAL INSTRUMENTS

Designing embedded-system applications with high-level tools

HIGH-LEVEL PROGRAMMING LANGUAGES HELP YOU MORE QUICKLY DEPLOY YOUR APPLICATION, BUT CAREFUL ATTENTION TO DETAILS CAN IMPROVE THE PERFORMANCE OF YOUR CODE AND LEAD TO AN EFFICIENT APPLICATION THAT YOU CAN STILL DEVELOP IN A TIMELY MANNER.

To meet time-to-market and productivity pressures, embedded-system developers increasingly consider and use high-level design-software tools that provide more abstraction, simpler representations of programming constructs, and automatic code generation. Embedded systems are generally restrictive, requiring a focus on execution speed, execution reliability, determinism, power consumption, and memory usage. To realize the promise of higher-level design software such as UML (Unified Modeling Language), National Instruments LabView, and frameworks such as Eclipse, designers must continue to pay attention to the challenges associated with embedded-system development. These higher-level design tools do not program themselves, and designers must continue to make trade-offs among factors including performance, memory usage, and power consumption. As a designer, you should evaluate the following development areas when using high-level design tools: memory usage and management, programming structures within embedded-system applications, processor-intensive calculations, and hybrid development—combining low- and high-level languages.

MEMORY MANAGEMENT

Applications that run solely on Windows rarely have to consider memory usage or management because Windows can access large amounts of virtual memory. However, an embedded-system application running on an RTOS (real-time operating system) does not use virtual memory because doing so hinders determinism. Also, when you restart an application in Windows, you "wipe clean" the application's memory, but in the RTOS, embedded-system applications start when you reset the real-time device and stop when you turn it off. Therefore, you should design your deterministic applications to be memory-conscious. For example, always preallocate space for your arrays equal to the largest array size that you will encounter (see **sidebar** "Data types and variables").

Proper memory allocation is a big part of efficiently programming embedded-system applications. In general, dynamic-memory allocation is an expensive operation that you should avoid. With dynamic-memory allocation, you can create data types and structures of any size and length to suit your program's needs. Dynamic-memory allocation differs from automatic or static-memory allocation and creates an object that remains allocated until the programmer or a garbage collector explicitly deallocates it.

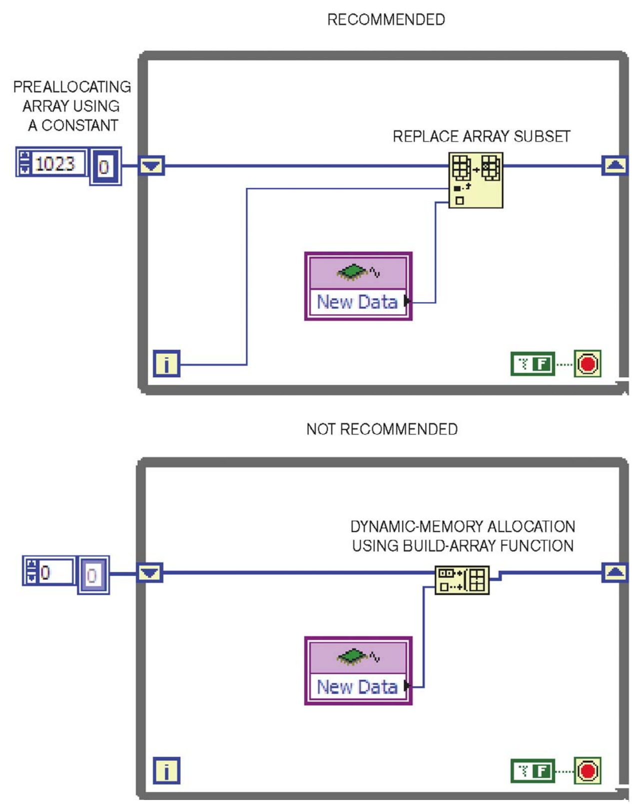


Figure 1 Dynamic-memory allocation is expensive in time-critical code. It is especially detrimental if dynamic allocation occurs inside a loop to store data in arrays. A common way to avoid dynamically allocating memory in a loop is to preallocate the memory for any arrays before the loop starts execution.

In general, dynamic-memory management is an important aspect of modern software-engineering techniques. However, real-time-system developers avoid using it because they fear that the worst-case execution time of the dynamic-memory-allocation routines is not bounded or has an excessively large bound. The following section highlights two examples—in C and in a higher-level graphical language, such as LabView.

In C, programmers most commonly use the function "malloc" to attempt to "grab" a continuous portion of memory and define it by: void *malloc(size_t number_of_bytes). Therefore, the function returns a pointer of type void * that is the start in memory of the reserved portion of sizeof() number_of_bytes. If the system cannot allocate memory, it returns a NULL pointer. Because it returns a void *, the C standard states that you can convert this pointer to any type. The size_t argument type is defined in stdlib.h and is an unsigned type.

Therefore, char *cp; cp=malloc(100) attempts to get 100 bytes and assigns the start address to cp. Also, it is common to use the sizeof() function to specify the number of bytes: int *ip; ip=(int *) malloc(100*sizeof(int)).

Some C compilers may require you to cast the type of conversion. The (int *) defines coercion to an integer pointer. Coercion to the correct pointer type is crucial to ensure that you correctly perform pointer arithmetic. It is beneficial to use sizeof() even if you know the size you want; it makes for device-independent—that is, portable—code.

In a graphical programming language such as LabView, dynamic-memory allocation can occur when using the build-array and concatenate-string functions. Alternatively, you can replace the build-array primitive with a replace-array-subset function to replace elements in a preallocated array. You should create the preallocated array outside the loop by using an array constant or the initialize-array function. See the LabView code in **Figure 1**, which compares the implementations.

TABLE 1 SAMPLE SCALING, MULTIPLIER, AND BIT-SHIFT VALUES

Desired scaling value	Multiplier	Bit shift	Actual scaling value	Absolute error
1.5	3	−1	1.5	0
0.1428	73	−9	0.1425	0.0003
10	3	−5	0.09375	0.00625
10	102	−10	0.09961	0.00039

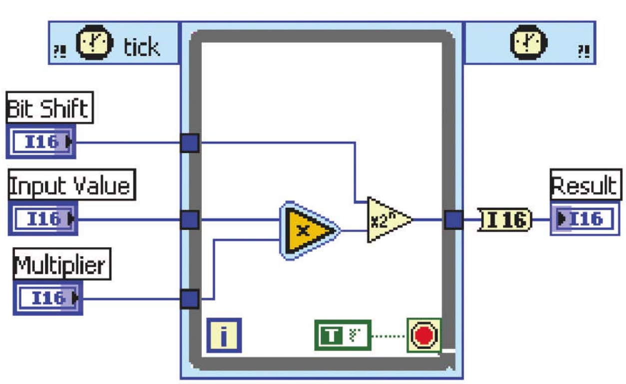


Figure 3 Designers can use the Embedded LabView FPGA virtual instrument to scale by a noninteger value.

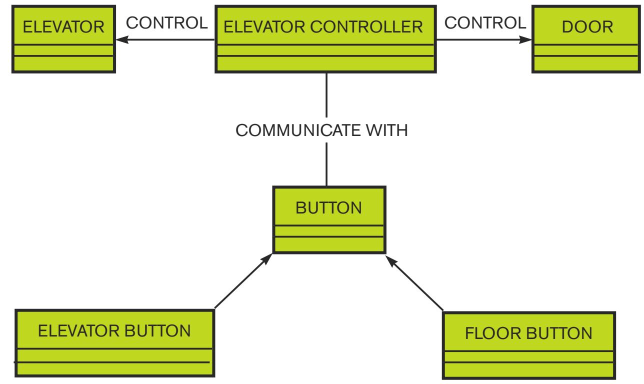


Figure 2 UML case diagrams show the static structure of an object, the internal structure, and relationships.

EMBEDDED-PROGRAMMING STRUCTURES

Engineers commonly use programming structures, such as for loops, while loops, and others, and case structures in desktop applications, but you should also review and optimize these structures for embedded-system applications. Each structure has its own use. At a simple level, if you know how many times you need to loop, then use a for loop. If you want to loop until the system meets a certain condition, then use a while loop. However, note that, whatever you can do with a for loop, you can do with a while loop; the number of loops can also be a condition. And, although you can use a while loop for anything a for loop can do, it's often recommended to use for loops instead of while loops because for loops have memory optimizations such that, if you know the number of iterations, you could preallocate the array. For embedded-system applications, there are a few more cases to avoid or consider when using programming structures.

Depending on the compiler, a constant inside a loop can cause each loop iteration to make a copy of that data, resulting in increased execution time and memory usage. You can avoid this situation either by moving the constant outside the loop or by using local variables to pass data into the loop. Therefore, avoid placing large constants inside loops. When you place a large constant inside a loop, the system allocates memory and initializes the array at the beginning of each loop iteration. This operation can be expensive in time-critical code. A better way to access the data is to place the array outside the loop and wire it through a loop tunnel, or you can use a global variable.

For simple decision-making, it is often faster to use the select function instead of a case structure. Because each case in a case structure can contain its own block diagram, there is significantly more overhead associated with this structure than with a select function. However, it is sometimes more optimal to use a case structure if one case executes a large amount of code and the other cases execute little code (**Figure 2**). You should decide whether to use a select function versus a case structure on a case-by-case basis.

Structs in C and clusters in LabView are useful for bundling heterogeneous data into manageable packages. However, information about the contents must also propagate with that data. Especially when passing data to subfunctions, individual

Agilent 34970A & 34980A switch/measure units

More measurements. More data. Less cost.

With up to 560 channels of data logging at a maximum scan rate of 1000 channels/sec, an internal 6 ½ digit DMM with 22-bit resolution, and 0.03% accuracy, it's no mystery why Agilent's data acquisition systems are among the top selling in the world. The 34970A and 34980A are both at home with either data acquisition or functional test, with a broad selection of plug-in modules.

Now with Agilent Data Logger Pro software, you'll be able to collect data, check limits, perform extensive branching, and view and store the data without authoring the programming yourself. It's an ideal expansion at a significant savings.

FREE Agilent Data Logger Pro software
a $795 - $995 value until 15 Oct 2008

u.s. 1-800-829-4444 canada 1-877-894-4414 www.agilent.com/find/daqpromo

Agilent Authorized Distributors

RS ELECTRONICS	*Allied Electronics*	*Hensley Technologies*	*Instrument Engineers*
888-852-7234	800-433-5700	877-595-7447	800-444-6106

Agilent Technologies

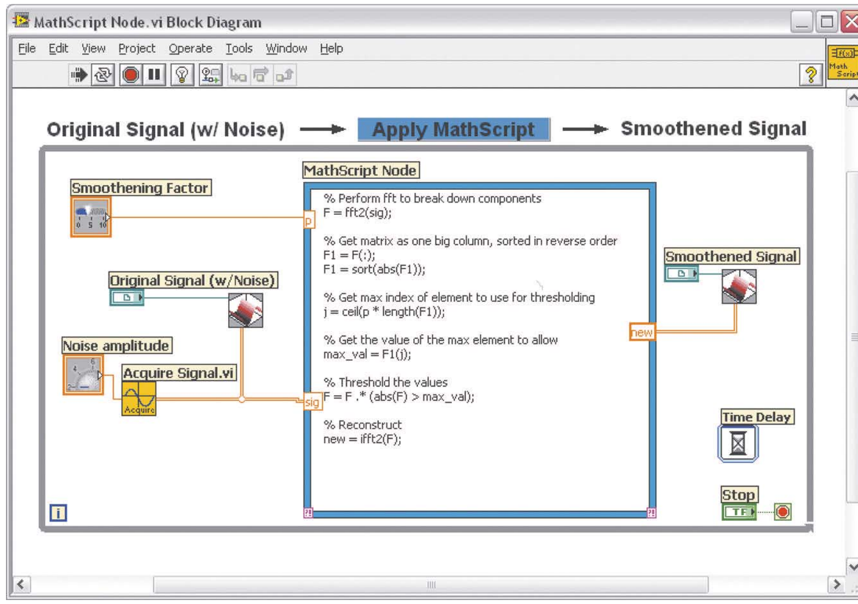


Figure 4 Graphical programming allows you to combine textual m-file-based mathematics plus C, assembly, or VHDL code into your designs.

elements rather than structs or clusters usually increase the speed of your applications. Use them to avoid passing unnecessary data-type information to the subfunction. The performance of passing a cluster or struct depends a lot on how you pass the information. For example, in C, you could pass the structure "in place"—that is, by pointer—and get good performance, possibly better than passing the individual elements, depending on the use case.

PROCESSOR-INTENSIVE MATH

You also have to consider the types of calculations you are performing to optimize your application. Some calculations, for example, are "processor-intensive" tasks. In general, a processor-intensive task is any task that is limited by how fast the processor can compute the data. Video encoding is an example of a processor-intensive application; I/O-bound tasks are more memory-intensive.

A more common way to optimize an application is through its calculations. A binary shift is one such optimization technique. In C programming, the operators for binary shifting are << and >>. Shifting to the left causes numbers to multiply by the power of two that you shifted them. Shifting to the right is identical, except it divides by the power of two.

For example, suppose you want to plot a pixel in VGA mode 13h by copying the color to the screen offset x+y×320. Because 320 is the same as 64+256, you can use screen[((y<<8)+(y<<6))+x]=color instead of screen[y×320+x]=color. This approach is much faster than multiplication, a complex operation, because binary shifts are simple operations. Handling scaling in the LabView FPGA tool is similar: Just use a multiply function and then a scale-by-power-of-two function. First, multiply the input value by a known integer, generating a larger intermediate result. Shifting the intermediate result to the left (scale-by-power-of-two function with a negative n value) is effectively a division by a power of two. Combining the multiplication and division gives the effective scaling or multiplication of the input value by a noninteger value. **Figure 3** shows an example of this scaling implementation. You can further optimize the code by replacing the bit-shift control with a constant.

As part of these calculations, it is important to make sure that the intermediate result of the multiplication fits into the data type you are using. With the saturation-multiply function, you can multiply two 16-bit integers, generate a 32-bit value, and know that the result fits into the 32-bit integer. If the final result needs to be a 16-bit integer, then the scale-by-power-of-two function must shift the intermediate product back into the 16-bit range with the coerce function (**Figure 3**). The integer multiplier and bit-shift value determine the noninteger-scaling value by which you are multiplying the input value. For example, to scale by 1.5, set the multiplier to 3 and the bit shift to −1. This step leads to 3/2, which equals 1.5. To scale by 1/7 (~0.1428), set the multiplier to 73 and the shift to −9. This step leads to 73/512, which equals approximately 0.1425.

Combining a multiplication and a scale-by-power-of-two function does not provide an exact result for every noninteger-scaling value, but it does offer a good approximation within the limited resolution of integers. The key is to find the right combination of multiplier and bit-shift value. For example, to divide by 10, you can use a multiplier of 3 and bit shift of −5 (divide by 32). Doing so results in an effective scaling constant of 3/32, which equals 0.09375, an error of 0.00625 from your intended value. However, you could also use a multiplier of 102 and a shift of −10 (divide by 1024), which gives you an effective scaling constant of 102/1024, approximately equal to 0.09961, an error of 0.00039 from your intended value. In general, you achieve better results when you use larger multipliers and bit-shift values.

As you increase the multiplier, make sure that you do not exceed the range of the intermediate-result data type; otherwise, you will saturate this value and receive an incorrect result. To find the right multiplier and bit-shift values, it is often easiest to pick a suitably large bit-shift value that you base on the output-

MORE AT EDN.COM

+ Go to www.edn.com/ms4248 and click on Feedback Loop to post a comment on this article.

DATA TYPES AND VARIABLES

Some environments automatically handle data-type conflicts by converting the smaller data type into the larger one. For example, if a type conflict exists between an integer and a floating-point number, your programming language may convert the integer into a floating-point number and then perform the operation. This conversion is expensive and, in many cases, unnecessary. In most cases, you can avoid casting and coercion by using the correct data type for each variable. However, if the data must be cast or coerced, it can be more efficient to convert the data before sending it to the operation or function.

For this discussion, it is best to establish some definitions to make sure your programmers are speaking the same language. Wikipedia defines a global variable as "a variable that does not belong to any subroutine or class and can be accessed from anywhere in a program." Likewise, a local variable is "a variable that is given local scope. Such variables are accessible only from the function or block in which [they are] declared."

In general, you can modify global variables from anywhere within the application; however, using global variables is a poor programming technique. A global variable has unlimited potential for creating mutual dependencies, and adding mutual dependencies increases complexity. Another challenge of using global variables is their associated complexity with code reuse because of the interdependencies.

Local variables, on the other hand, can have a scope that is declared, written to, and read, usually with no side effects–except if your variable data is bound to the user interface. For example, with National Instruments' LabView, every time you access a local variable, it executes extra code to synchronize the variable with the user interface or front panel. You can improve code performance, in many cases, by using a global variable instead of a local variable. The global variable has no extra front-panel synchronization code. Therefore, globals of 8 bytes or less are faster than local variables. If a global is larger than 8 bytes, you cannot access it atomically, and it requires a mutex, making it slower and making it a shared resource.

YOU OFTEN OBTAIN THE BEST RESULTS BY USING A HYBRID OF HIGH- AND LOW-LEVEL CODE.

value range and data types and then calculate the corresponding multiplier for your desired scaling value. Also, by using a constant value for the bit shift, you use fewer resources on the FPGA when compiled. **Table 1** shows sample scaling values and the corresponding multiplier and bit-shift values.

For processors with no floating-point units, converting to floating point to perform an operation and then converting back to an integer data type can be expensive. For example, using a quotient-and-remainder function is faster than using a normal divide function, and using a logical-shift function is faster than using a scale-by-power-of-two function.

Integer-math routines available on fixed-point platforms, such as an FPGA, make data processing a little more challenging. You can use integer-math functions to scale or multiply data by whole integer values. You can use bit shifting to multiply or divide a value by any power of two. When you combine these two operations, you create a simple method to scale or multiply a value by a noninteger scaling constant.

A common application of scaling an input value by a constant is in simulators of sensors, such as LVDTs (linear-variable-differential transformer) and synchro/resolvers. Each of these sensors has an excitation-voltage input that a sine-wave signal feeds. The sensor modulates the amplitude of the excitation signal based on the position of the sensor, and the system passes the resulting output signal to the measurement system. When you want to simulate such a sensor, you need to measure the excitation signal and generate an analog-output value that corresponds to the excitation voltage scaled by a value corresponding to the position of the simulated sensor. This operation requires you to quickly multiply the analog-input measurement by a noninteger value and generate the result on an analog-output channel.

You often obtain the best results by using a hybrid of high- and low-level code. With many high-level, open programming languages, you can use C or assembly code directly within your application. It is best to use low-level algorithms within your code if you want to reuse algorithms or if there is a small numeric or array algorithm you can code more optimally. LabView uses a graphical-system-design approach that encompasses many models of computation. You can combine textual m-file-based mathematics with graphical programming; insert C, assembly, or VHDL code into your designs; and access models such as state and simulation diagrams (**Figure 4**). Therefore, you can choose the right approach for each unique challenge you are trying to solve. You must also emphasize the importance of performance profiling. Make sure that you spend time optimizing the 20% of the code that takes 80% of the time. This 20/80 pattern is extremely prevalent, yet programmers too often spend hours unnecessarily fine-tuning the 80% of their code that does not significantly affect performance.

By following good embedded-programming practices, you can better optimize your code to meet the constraints of your embedded-system application. Implementing one or two of these techniques may noticeably improve the performance of your application, but the best approach is to incorporate a combination of all these techniques.EDN

AUTHOR'S BIOGRAPHY

Shelley Gretlein is a real-time- and embedded-product strategist at National Instruments, where she works with real-time and embedded hardware and software products, including LabView Real-Time, LabView FPGA, LabView Embedded, and LabView control design and simulation, as well as hardware targets, including CompactRIO and PXI. She also evaluates future technologies for upcoming product integration, including RTOSs, FPGAs, and general software technologies. Gretlein holds bachelor's degrees in computer science and in management systems from the University of Missouri—Rolla. She enjoys wakeboarding, running, triathlons, and renovating.

LINEAR TECHNOLOGY
DESIGN NOTES

µModule LED Driver Integrates All Circuitry, Including the Inductor, in a Surface Mount Package – Design Note 445

David Ng

Introduction

Once relegated to the hinterlands of low cost indicator lights, the LED is again in the spotlight of the lighting world. LED lighting is now ubiquitous, from car headlights to USB-powered lava lamps. Car headlights exemplify applications that capitalize on the LED's clear advantages—unwavering high quality light output, tough-as-steel robustness, inherent high efficiency—while a USB lava lamp exemplifies applications where *only* LEDs work. Despite these clear advantages, their requirement for regulated voltage *and* current make LED driver circuits more complex than the venerable light bulb, but some new devices are closing the gap. For instance, the LTM®8040 µModule™ LED driver integrates all the driver circuitry into a single package, allowing designers to refocus their time and effort on the details of lighting design critical to a product's success.

A Superior LED Driver

The LTM8040 is a complete step-down DC/DC switching converter system that can drive up to 1A through a string of LEDs. Its 4V to 36V input voltage range makes it suitable for a wide range of power sources, including 2-cell lithium-ion battery packs, rectified 12VAC and industrial 24V. The LTM8040 features both analog and PWM dimming, allowing a 400:1 dimming range. The built-in 14V output voltage clamp prevents damage in the case of an accidental open LED string. The default switching frequency of the LTM8040 is 500kHz, but switching frequencies to 2MHz can be set with a resistor from the RT pin to GND.

Easy to Use

The high level of integration in the LTM8040 minimizes external components and simplifies board layout. As shown in Figure 1, all that is necessary to drive an LED string up to 1A is the LTM8040 and an input decoupling capacitor. Even with all this built-in functionality, the LTM8040 itself is small, measuring only 15mm × 9mm × 2.82mm.

Rich Feature Set

The LTM8040 features an ADJ pin for precise LED current amplitude control. The ADJ pin accepts a full-scale input voltage range of 0V to 1.25V, linearly adjusting the output LED current from 0A to 1A. Figure 2 shows the ratiometric response of the output LED current versus the ADJ voltage. The ADJ pin is internally pulled up through a 5.11k precision resistor to an internal 1.25V reference, so the output LED current can also be adjusted by applying a single resistor from ADJ to ground, as shown in Figure 3.

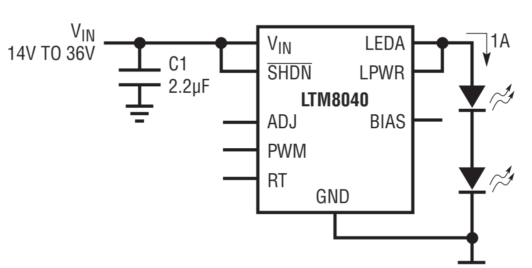


Figure 1. Driving an LED String with the LTM8040 Is Simple—Just Add the Input Capacitor and Connect the LED String

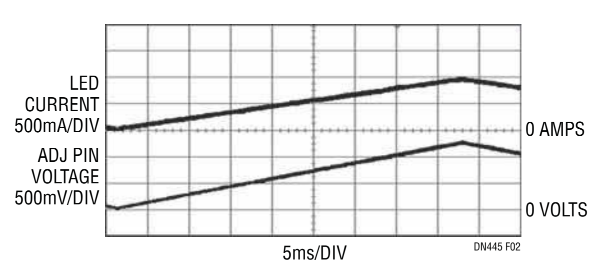


Figure 2. Drive a 0V to 1.25V Voltage into the ADJ Pin to Control the LED Current Amplitude

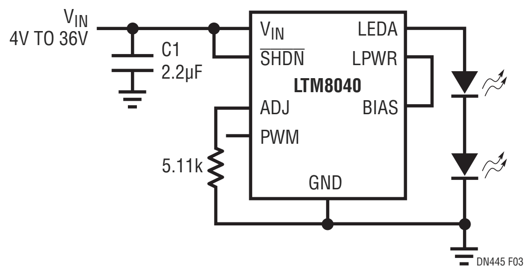


Figure 3. Control the LED Current with a Single Resistor from ADJ to Ground

The PWM control pin allows high dimming ratios. With an external MOSFET in series with the LED string as shown in Figure 4, the LTM8040 can achieve dimming ratios in excess of 400:1. As seen in Figure 5, there is little distortion of the PWM LED current, even at frequencies as low as 10Hz. The 10Hz performance is shown to illustrate the capabilities of the LTM8040—this frequency is too low for practical pulse width modulation, being well within the discrimination range of the human eye.

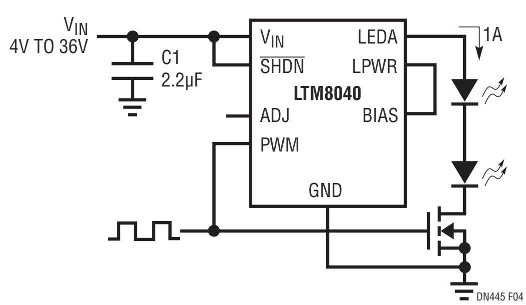


Figure 4. The LTM8040 Can PWM its LED String with an External MOSFET

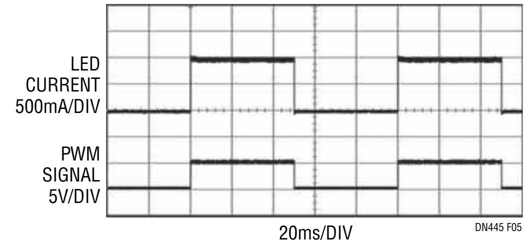


Figure 5. The LTM8040 Can PWM LED Current with Minimal Distortion, Even at Frequencies as Low as 10Hz

The LTM8040 also features a low power shutdown state. When the SHDN pin is active low, the input quiescent current is less than 1µA.

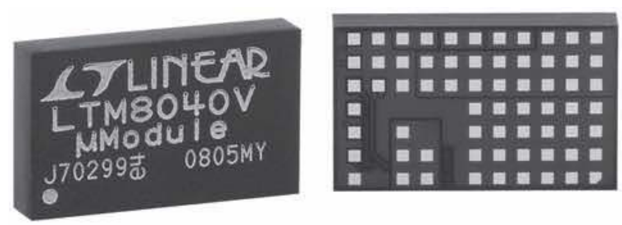


Figure 6. Only 9mm × 15mm × 2.82mm, the LTM8040 LED Driver is a Complete System in an LGA Package

Conclusion

The LTM8040 µModule LED driver makes it easy to drive LEDs. Its high level of integration and rich feature set, including open LED protection, analog and PWM dimming, save significant design time and board space.

Data Sheet Download

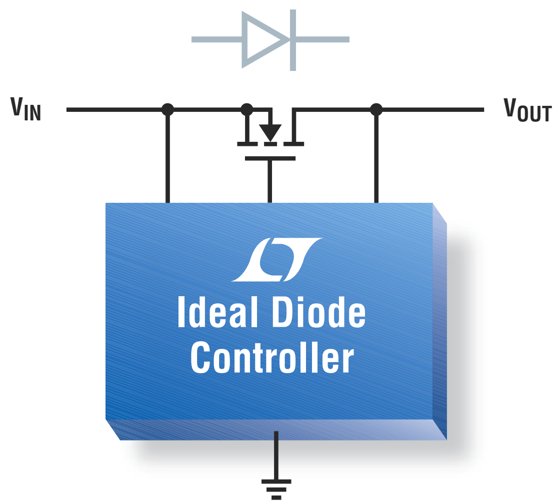
www.linear.com, see also www.linear.com/micromodule

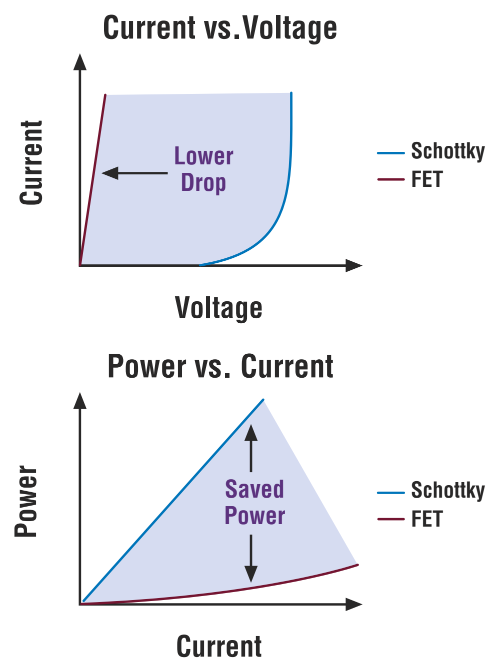
For applications help,
call (408) 432-1900, Ext. 2593

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com

dn445f LT/TP 0708 392K • PRINTED IN THE USA

Are Your Diodes Ideal?





Our Controllers Turn MOSFETS into Ideal Diodes with Lower Voltage Drop, Less Power Loss & Reduced Heatsinking

Our Ideal Diode controller family reduces forward voltage drop and power dissipation in ORing applications, eliminating the heatsinks required by conventional rectifiers. They deliver smooth switchover without chatter, are free from oscillation in load-sharing applications, yet respond quickly when needed to block DC current in the reverse state. Our controllers prevent back-feeding between supplies and are easily configured to protect against reverse polarity inputs.

Family of High Voltage Diode Controllers

Part No.	Input Supply Range	Ideal Diode	Fault Monitoring	Package (mm)	Applications
LTC®4354	−4.5V to −80V	Dual	Yes	2 x 3 DFN-8, SO-8	−48V Distributed Power Systems AdvancedTCA Systems N+1 Redundant Power Supplies High Availability Systems Telecom Infrastructure Automotive Systems Optical Networks
LTC4355	9V to 80V	Dual	Yes	3 x 4 DFN-14, SO-16	
LTC4357	9V to 80V	Single	No	2 x 3 DFN-6, MSOP-8	
LT®4351	1.2V to 18V	Single	Yes	MSOP-10	

Info & Free Samples

www.linear.com/idealdiodes

1-800-4-LINEAR

Free Telecom, Datacom and Industrial Brochure

www.linear.com/48vsolutions

LINEAR TECHNOLOGY

Low-cost circuit incorporates mixing and amplifying functions

Guus Colman, Guy Torfs, Johan Bauwelinck, and Jan Vandewege,
INTEC/IMEC, Ghent University, Ghent, Belgium

In many applications, the frequency-conversion steps comprise a buffer, preferably with some extra voltage gain; a mixer; and some filtering. Instead of including an amplifier in front of the mixer, you can easily integrate the mixer function with the amplifier. A low-cost implementation uses an amplifier with a power-down-disable feature. When a square-wave local oscillator drives the disable pin, a square wave at the oscillator's frequency multiplies the input signal, and frequency conversion takes place.

The circuit in **Figure 1** uses an Analog Devices (www.analog.com) low-cost, 300-MHz, rail-to-rail AD8063 amplifier. The test circuit comprises a noninverting-op-amp circuit, which drives a load of 4 kΩ. The two resistors in the feedback loop regulate the voltage-conversion gain. In the test circuit, the voltage gain is 20 dB. However, you must consider the switching loss, which is about 10 dB when using an ideal switch and a 50%-duty-cycle clock. This scenario results in a 10-dB voltage-conversion gain.

Because the switching interrupts the power-supply current, the device's turn-on and turn-off times have a nonnegligible influence on conversion gain and nonlinearities. The AD8063's turn-on time, at 40 nsec, is less than the turn-off time of 300 nsec. In these cases, more signal power passes to the output, which results in an increase in voltage-conversion gain. **Figure 2** shows the voltage-conversion gain of the test circuit when downconverting an input signal to 12 kHz with a local-oscillator duty cycle of 50%. You can easily adjust this conversion gain by changing the two resistors in the feedback loop.

Another aspect of a mixer's ac performance is distortion. The test circuit maintains a second-order harmonic distortion of 35 dB and a third-order harmonic distortion of 43 dB when mixing a 5-MHz signal to a 12-kHz, 1V-p-p output signal. The circuit can downconvert two sine waves of identical power at 5 and 5.002 MHz to 12 and 14 kHz, respectively, with an intermodulation distortion of 47 dB. EDN

DIs Inside

What are your design problems and solutions? Publish them here and receive $150! Send your Design Ideas to edndesignideas@reedbusiness.com.

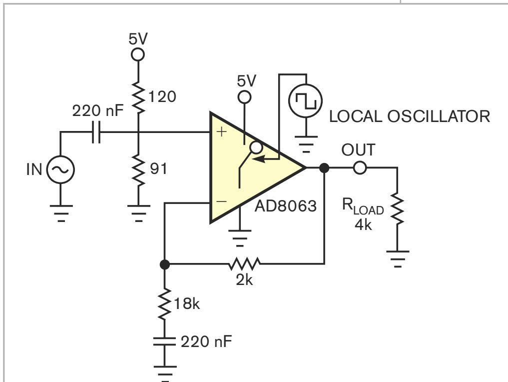


Figure 1 This circuit integrates the mixer function with a noninverting amplifier. The two resistors in the feedback loop set the voltage-conversion gain.

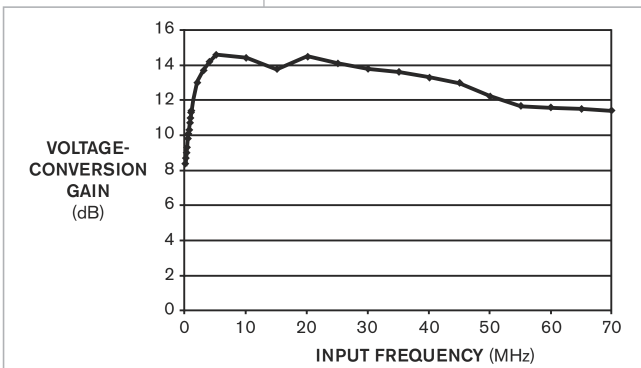


Figure 2 This graph shows the voltage-conversion gain of the test circuit when downconverting an input signal to 12 kHz with a local-oscillator duty cycle of 50%. You can easily adjust this conversion gain by changing the two resistors in the feedback loop.

Simple blown-fuse indicator sounds an alarm

Vladimir Oleynik, Moscow, Russia

Safety fuses or fusible links see wide use in modern electronic equipment to protect the load and the power supply—especially batteries—against short circuits and excessive load current. Fuses are inexpensive and simple, and a wide range of parts is available. However, you must replace them when they blow, and, when they do, you need an indicating circuit that warns you about its failure, especially when the fuse body is ceramic or sand-filled for improved protection against arcing.

The circuit in **Figure 1** signals that a fuse has blown. Input voltage ranges from 4 to 30V dc. The input range of the 78L05 voltage regulator determines the high limit; the lower one is less than the input range of the voltage regulator, but 4V dc is sufficient for the indicator to operate.

When fuse F_1 is in good order, diode D_1 is forward-biased, but its forward voltage is insufficient to bias forward-flashing diode D_2 and the Q_1's base-emitter junction. The self-driven HCM1206X buzzer is off, and the flashing diode does not flash. So, the alarm circuit is in standby mode. When F_1 blows, it no longer bridges the base-emitter-flashing-LED network. The 1-kΩ resistor forward biases D_2 and Q_1's base-emitter junction, forcing the buzzer to sound at a low frequency equal to the flashing frequency of D_2. During circuit operation, the 0.1-μF capacitor eliminates the buzzer's "tinkling" when the flashing LED is in the off state. **EDN**

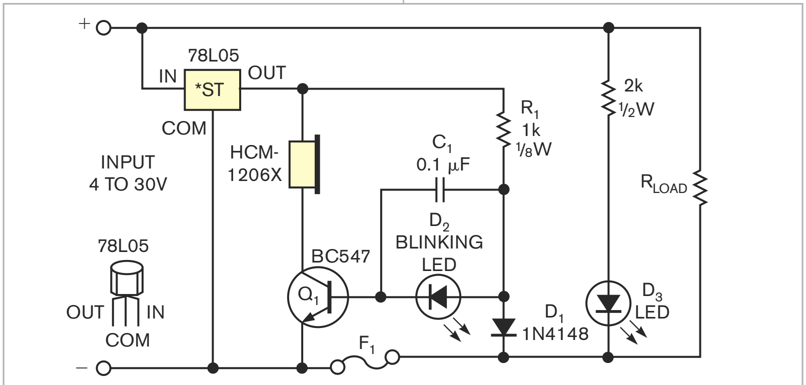


Figure 1 When fuse F_1 blows, the transistor biases on, sounding the buzzer and powering D_2.

Tester cycles system-power supplies

Goh Ban Hok, Infineon Technologies Asia Pacific Ltd, Singapore

Power-cycle testing is important because it tests the user environment. A poorly designed system board or chip can cause the power-cycle testing to fail, however. What's more, the power-cycle-test setup for system-board bench testing could require the use of a bulky and expensive commercial power supply. The situation gets worse when you need to simultaneously test several system boards.

This Design Idea describes a simple and inexpensive power-cycle circuit using just a few components (**Figure 1**). The power-supply input voltage is a dc supply from an inexpensive switching-power-supply adapter. This type of power adapter normally provides power for the system board. The circuit uses a 12V supply. You plug the power jack of the power unit into power socket J_1. The output voltage of this circuit from socket J_2 then connects to the system board to perform the power cycling. The 12V supply passes through resistors R_5 and R_6, which limit the current flowing through relay switches S_1 and S_2.

During start-up, the contact of relay S_2 is normally closed, allowing the 12V supply coming from R_6 to pass to resistors R_1 and R_2 and charge up capacitor C_1. Resistor R_8 in series with transistor Q_2 increases the charging and discharging duration of capacitor C_1. Transistor Q_2 turns on once capacitor C_1 charges toward 2V. This action impresses approximately 0.7V across the base-emitter voltage of transistor Q_2, which turns on Q_2. When transistor Q_2 turns on, it provides a low-resistance path for the coil of S_2 and thus energizes the relay, causing S_2's contact, 2_B, to close.

THIS DESIGN IDEA DESCRIBES A SIMPLE AND INEXPENSIVE POWER-CYCLE CIRCUIT USING JUST A FEW COMPONENTS.

When this scenario occurs, the 12V power supply switches its path to contact 2_B and enables the optocoupler's diode to conduct, turning on its internal transistor. The optocoupler then drives transistor Q_1. When Q_1 turns on, it provides a path for the coil of S_1, which energizes and thus connects the 12V supply to the output voltage. The circuit connects the output voltage to the power supply of the system board, thus powering up the board.

The system board remains powered up for approximately 45 sec. During the on time, capacitor C_1 discharges slowly through R_2, Q_2, and R_8. C_1 turns off transistor Q_2 once the voltage across the base of the transistor is below the transistor's turn-on voltage. Then, contact 2_B connects to contact 2_A, and the cycle repeats.

The off time for this circuit should be approximately 17 sec. Freewheeling diodes D_1 and D_2 reduce the large transient voltages that occur when the currents through the relay coils change quickly. EDN

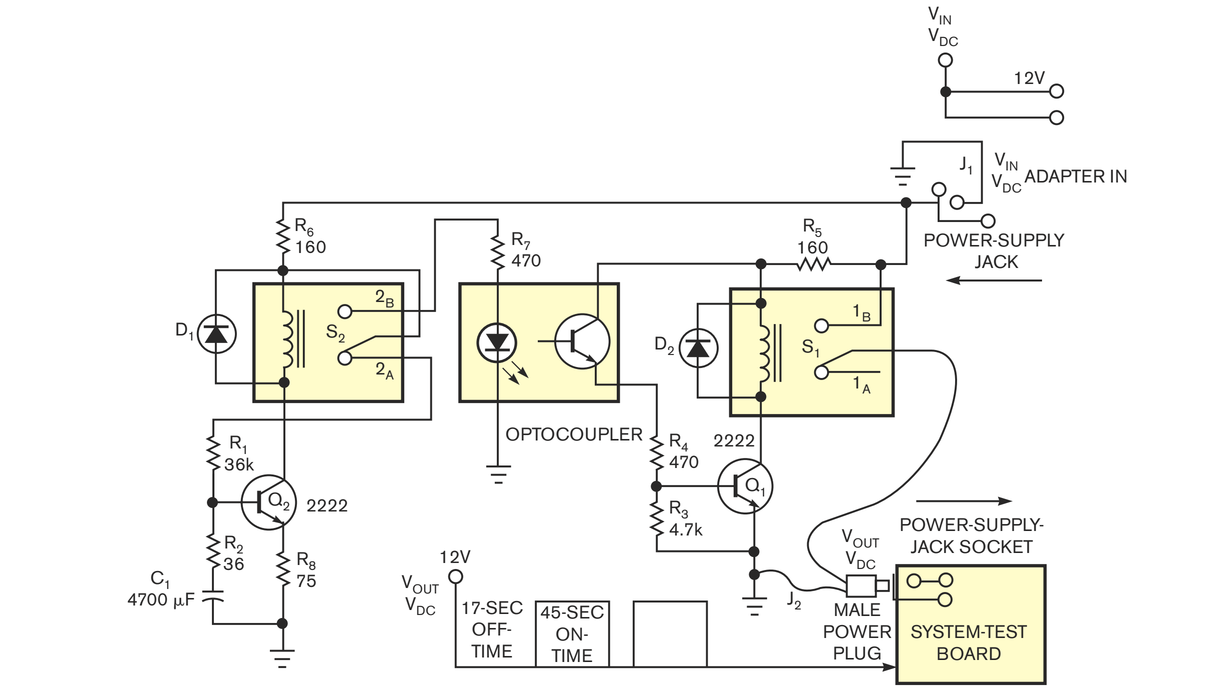


Figure 1 This simple and inexpensive power-cycle circuit uses just a few components.

Touch-activated timer switch extends battery life

Israel Schleicher, Prescott Valley, AZ

A certain type of cordless optical computer mouse operates on two AA alkaline cells. It has no power on/off switch. When not in use, it automatically reduces power consumption by switching its light source on and off at a low duty cycle. Nevertheless, this function unnecessarily drains the battery, and it is annoying to often find the device inoperable. The solution to the problem is to add a battery switch that automatically disconnects the battery after a preset time. This approach requires no disassembly or other kind of tampering. This Design Idea describes two distinct implementations of a touch-activated timer switch that you can add to many battery-operated gadgets that you might inadvertently leave on.

The circuit in **Figure 1** illustrates an analog implementation of the switch. **Figures 2** and **3** show digital implementations. The idea is to insert a 30-mil-wide strip of dual-sided PCB (printed-circuit board) between the negative pole of the battery and the spring contact of the battery holder (Item A in the **figures**). Q_3 is a low-threshold MOS transistor that connects between the two sides of the strip and serves as the switching element (**Figure 1**). C_1 is a 0603 X7R ceramic-chip capacitor, and R_1 is a 0603 chip resistor. You mount Q_3 and all associated components near the upper edge of Item A. You insert a narrow strip of thin brass, Item B, in series with the positive pole of the second cell. You connect it to the circuit with a piece of thin, flexible wire. Touch contacts C and D comprise short strips of self-adhesive copper tape that you attach outside the battery compartment. Thin and flexible wires connect C and D to the circuit.

THIS DESIGN IDEA DESCRIBES A TOUCH-ACTIVATED TIMER SWITCH THAT YOU CAN ADD TO MANY BATTERY-OPERATED GADGETS.

Q_1, Q_2, and C_1 form a monostable flip-flop. When the switch is off, C_1

does not charge, and both Q_1 and Q_2 are off. When you momentarily touch both C and D with bare fingers, current through your hand charges C_1 to the threshold level of Q_2. Both Q_2 and Q_1 turn on, discharging C_1 through Q_1 and your conductive fingers. The voltage level at the gate of Q_2 is then close to the battery voltage. After you remove your fingers, the leakage through the internal gate protection of Q_2—the zener diode in the **figures**—causes the voltage at the gate of Q_2 to slowly drift lower until it reaches the threshold level of approximately 1.3V. Q_2 exits conduction and, with Q_1, causes a regenerative action to quickly turn off Q_3.

The switch remains off until you again touch C and D. Item E is an optional contact similar to C and D. If you touch E and D, the switch turns off. Using a value of 0.01 μF for C_1, you obtain a delay of approximately one hour. Because the gate leakage is on the order of a few picoamperes, you must clean the circuit with a flux solvent and then coat it with a drop of wax or epoxy resin.

In some cases, you might want to be able to adjust the timing of the switch. The circuit in **Figure 2** provides that option. It uses a tiny microcontroller in an SOT-23 package. **Listing 1**, which is available in the Web version of this Design Idea at www.edn.com/080710di1, contains the touch-activated timer switch. Items A, B, C, and D are the same as those in **Figure 1**. When the switch is off, the PIC10F200T microcontroller is in sleep mode and consumes practically no power. When you simultaneously touch contacts C and D, the level at Pin 1 of IC_1 goes high, and the microcontroller starts to tally the time that Pin 1 remains high. After 0.5 sec, the buzzer sounds a short beep. The buzzer then sounds two, three, and four fast beeps in 0.5-sec intervals. By immediately releasing contacts C and D after hearing any number of beeps, you can set the switch for 30 seconds, 30 minutes, four hours, and eight hours of operation, respectively. The choices of operating times are arbitrary; you can modify the code in **Listing 1** to whatever fits your application. Jump-

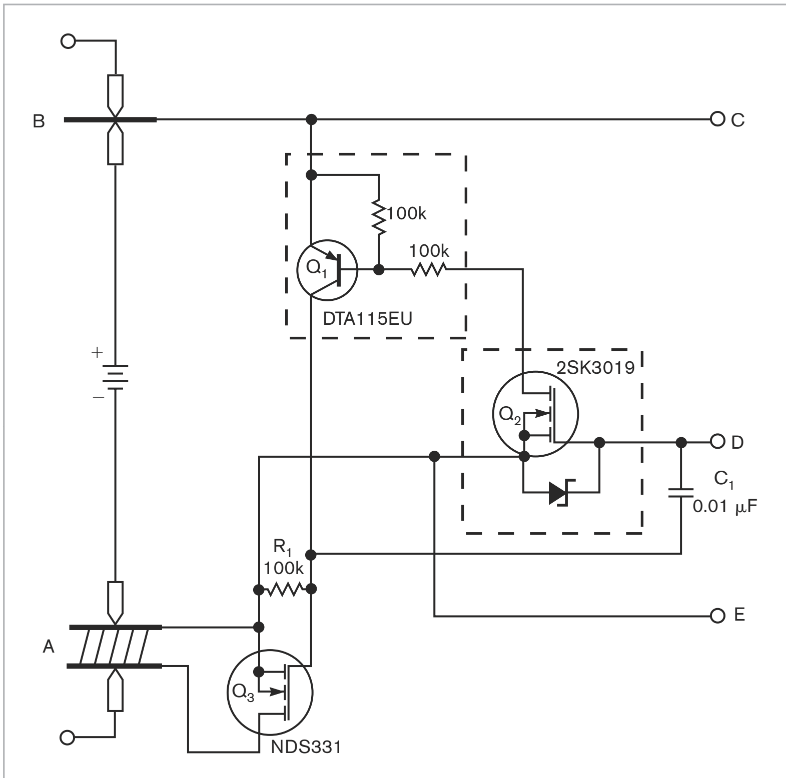


Figure 1 In parallel with the cells of a battery-powered device, this analog circuit disconnects the battery after a delay. Touching contacts C and D with a finger turns on the switch, connecting the cells to the load. The components fit inside the battery compartment.

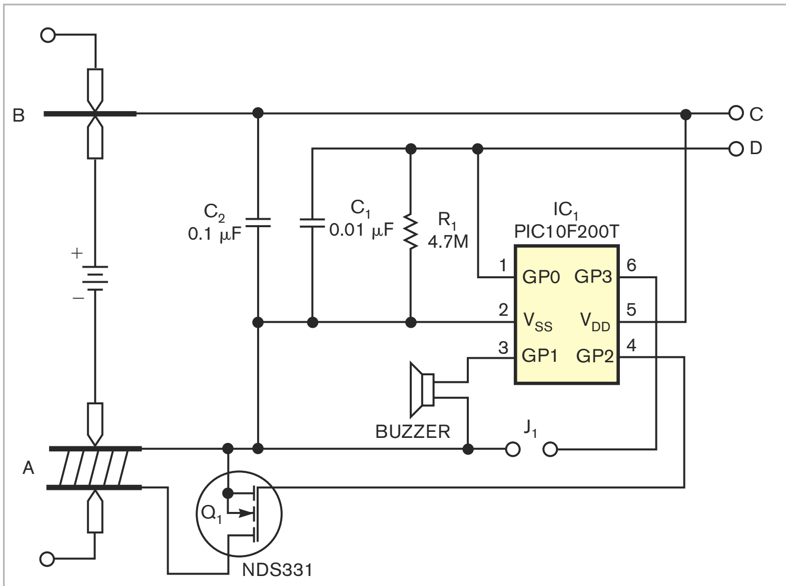
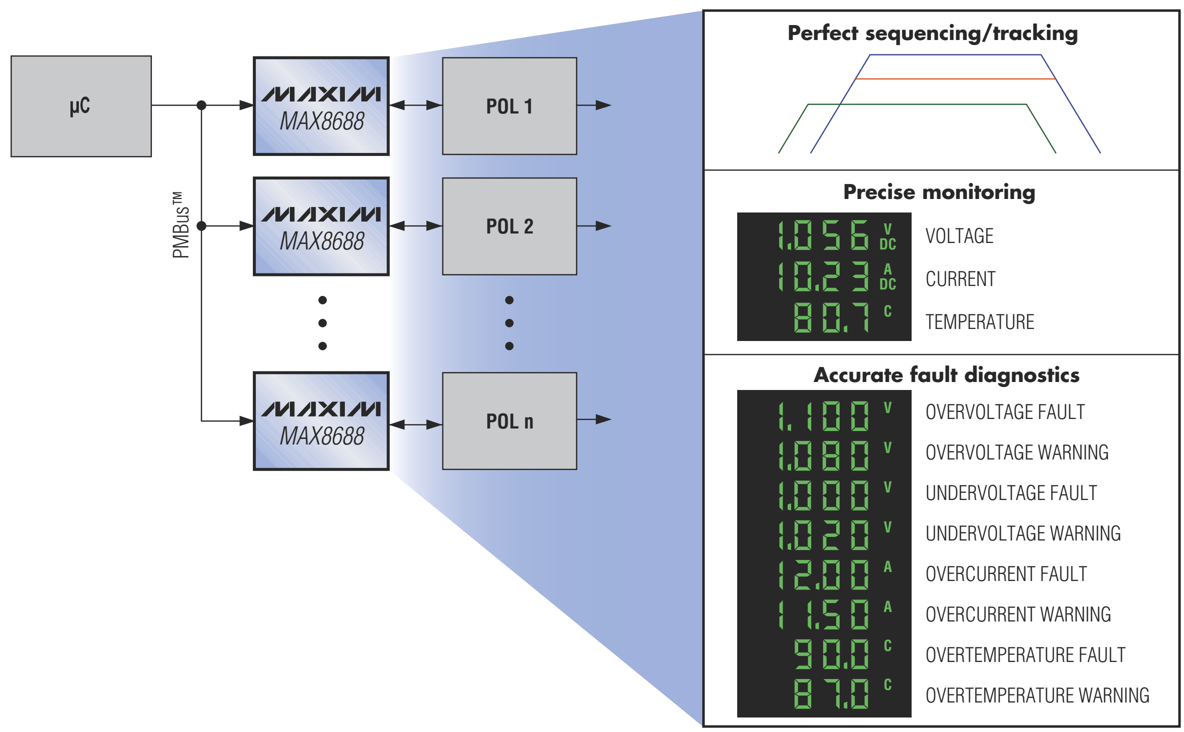


Figure 2 This digital implementation of the battery-disconnect switch uses a PIC10F200T microcontroller to control the disconnect switch.

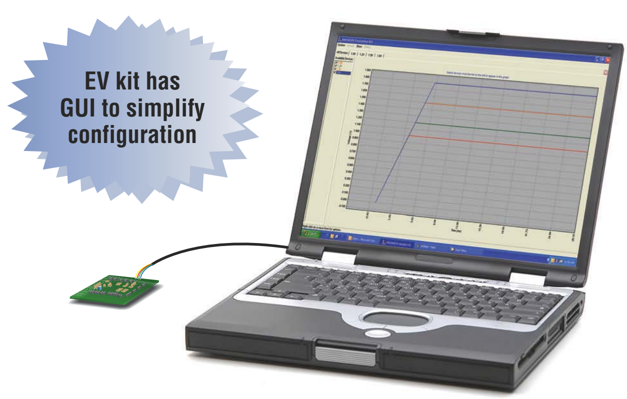
MAXIM 1983 • 2008 25 YEARS OF ENGINEERING SUCCESS

Add complete programmability and digital control to any POL power supply

PowerMind™ controller/monitor simplifies design, reduces cost, and provides unmatched accuracy



- Control up to 127 addresses on a single bus
- Closed-loop operation provides ±0.2% output voltage accuracy over temperature
- Accurate current monitoring
- PMBus compliant
- Data logging and fault diagnostic capabilities
- Small, 4mm x 4mm, 24-pin TQFN



PowerMind is a trademark of Maxim Integrated Products, Inc.
PMBus is a trademark of SMIF, Inc.

MAXIM DIRECT
www.maxim-ic.com/shop

AVNET electronics marketing
www.avnet.com

MAXIM
www.maxim-ic.com/MAX8688-info

For free samples or technical support: www.maxim-ic.com/support or 1-800-998-8800 er switch J_1 is optional. If you leave it open, touching C and D turns it off. Short-circuiting J_1 disables this option, and the switch will turn off only at the end of the programmed time. As is the case with the analog implementation, you mount all components except the buzzer at the edge of Item A. The buzzer is a small piezoelectric element with a resonant frequency of 4 kHz and can easily fit inside the battery compartment.

In some cases, you may not have access to the negative contact of the battery holder. The circuit in **Figure 3** addresses this situation. It is essentially the same as the circuit in **Figure 2**, except that you place Item A in series with the positive pole and attach B to the negative pole of the battery. A P-channel MOS transistor acts as a switch, and you modify the microcontroller's program to provide a low level to drive Q_1. A comment in **Listing 1** indicates the proper line of code for the options in either **Figure 2** or **Figure 3**.EDN

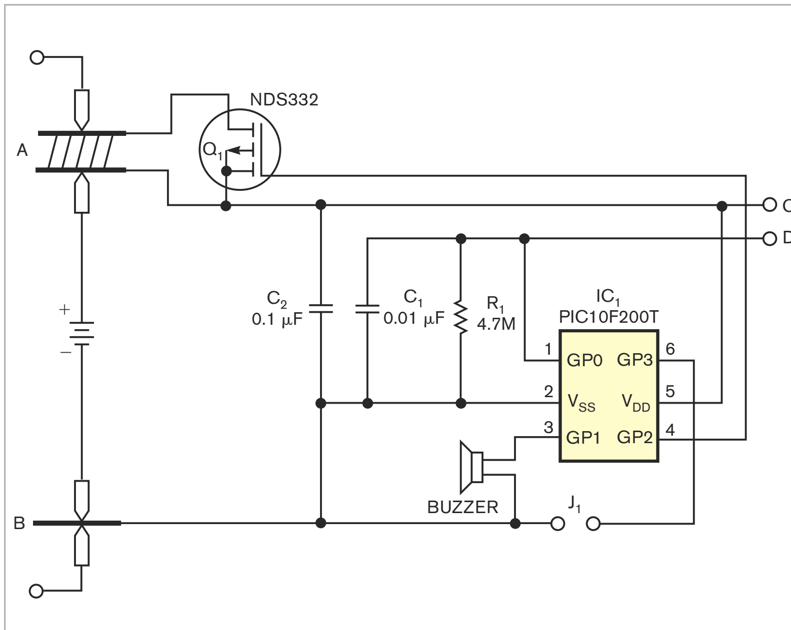


Figure 3 This circuit addresses the problem of a lack of access to the negative contact of the battery holder. It is essentially the same as the circuit in Figure 2, except that you place Item A in series with the positive pole and attach B to the negative pole of the battery.

productroundup

PASSIVES

Inductive families add a variety of inductors and chokes

The vendor's 10 inductive-component families aim at power and EMC-filtering applications. The family includes bobbin-wound, surface-mount inductors; vertical-mount, leaded-toroid inductors; low-profile, shielded and unshielded surface-mount inductors; flat-coil, surface-mount power inductors; and leaded common-mode chokes. The inductors have a −40 to +125°C temperature range; the range of common-mode chokes suits use at −40 to +85°C. Prices for the ROHS-compliant inductor series range from 30 cents to $1.40.

Murata Power Solutions, www.murata-ps.com

Rejustors suit extreme-temperature environments

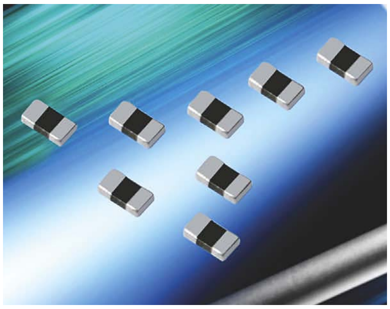
Suiting applications requiring precision and accuracy in extreme-temperature environments, the Type I and Type II rejustors operate over a −55 to +230°C extended-temperature range and claim a lifetime drift of less than 1%. The resistor element allows independent electrical adjustments to any value from the device's nominal to 80% of the nominal value. The Type I rejustors consist of a pair of nominally 27-kΩ rejustors, offering adjustments of less than 0.1% and maintaining a ±2.5% tolerance over the operating temperature. The Type II rejustors feature ±0.7% resistance tolerances and are tuned to a 50°C window or band within the temperature range. The HT-rejustor dividers provide temperature stability, allowing a ±1% ratio between the two resistors, regardless of the adjustment state of either HT rejustor if both devices are at the same temperature. The Type I, Type IIA, and Type IIB rejustors cost $6.95, $7.64, and $8.34 (1000), respectively.

Microbridge Technologies, www.mbridgetech.com

Miniature silicon-chip capacitor has low profile

The miniature, wire-bondable SiC0101 silicon-chip capacitor has a wire-bondable pad on the top and metallization on the back, allowing the use of epoxy die. The capacitor aims at RF-microwave, multichip-module, and hybrid-microelectronics applications. Sandwiched between two metal plates, the capacitor has a layer of silicon-nitride dielectric film providing a 4.7- to 22-pF capacitance. The vendor claims that the device has a frequency range of 1 MHz to several gigahertz. Measuring 0.25×0.25 mm, the capacitor comes as thin as 0.1 mm with additional thickness on the same footprint. Prices for the SiC0101 range from 1 to 2 cents (50,000), depending on capacitance value, tolerance, and chip thickness.

OnChip Devices, www.onchip.com



Less-than-1-pF multilayer varistor provides fast ESD response

Joining the vendor's low-capacitance MLV (multilayer-varistor) AntennaGuard Series, the less-than-1-pF version protects high-speed digital interfaces, RF antennas, and RF-

PASSIVES

amplifier circuits against ESD events. Providing a fast response time to ESD, the MLV withstands 1000 lightning strikes at 8 kV in accordance with the IEC 61000-4-2 standard. The new version includes a 0.8-pF capacitance at 10 and 15V rating in a 0402 case. The device costs 1 to 2.4 cents, based on application and volume.

AVX Corp, www.avx.com

Power resistors feature variety of TCR ratings

The CRCWxx-EL thick-film power resistor has a 10- to 100-mΩ resistance range with ±1 and ±5% tolerances. The resistor provides TCR ratings at ±100, ±200, ±300, ±400, and ±600-ppm/K over a −55 to +155°C temperature range. Meeting ROHS-compliant requirements, the resistor uses lead-free solder contacts on a nickel-barrier layer, with pure-tin plating, providing compatibility with lead-free and lead-containing soldering processes. Available in 0.1W 0603, 0.125W 0805, and 0.25W 1206 case sizes, the CRCWxx-EL power resistors cost 8 cents (1000).

Vishay Intertechnology, www.vishay.com

TEST AND MEASUREMENT

RF-test-instrument family adds WiMax testing

Adding to the vendor's RF-test capabilities, the 2820 and 2920 signal-creation and -analysis tools allow WiMax-signal testing. Built on a next-generation hardware platform, the tools add support for new signal standards, including the 802.16e mobile-WiMax Wave 2 testing with 4×4 MIMO channels, requiring no hardware upgrades or additional instruments. The instruments also support testing at frequency bands as low as 400 MHz, popular in new WiMax designs. The RF-test devices are based on

the vendor's Model 2820 RF-vector-signal analyzers and the Model 2920 RF-vector-signal generators. The 4-GHz 2820 and 2920 instruments cost $25,000 and $23,000, respectively. SignalMeister-specific software licenses cost $2500, and you can download free versions from the vendor's Web site.
Keithley Instruments, www.keithley.com

VXI-instrument card provides high stimulus accuracy

The DSP-based, single-slot 65-CS4 VXI card includes modular design, providing as many as four synchro/resolver instrument-grade measurement channels and as many as four synchro/resolver instrument-grade stimulus channels or as many as eight synchro/resolver embedded-grade stimulus channels and as many as six programmable-reference supplies. Features include a synchro/resolver instrument-grade measurement, 0.005° stimulus accuracy, and 0.015° embedded-grade stimulus accuracy. Instrument stimulus and reference outputs provide a 2.2-VA drive, and the device has a programmable 47- to 10,000-Hz range. The 65CS4 VXI card costs $10,000 (100).
North Atlantic Industries, www.naii.com

Module provides array of input- and output-analog-conversion combinations

The customizable DR900 universal signal-conditioning module provides more than 100 input- and output-analog-conversion combinations and three-way signal isolation. Factory precalibrated for all input and output ranges, the module allows factory or custom field scaling using an easy-mode switch change. Available in linear or square-root-extraction models, the DR900 universal signal-conditioning module costs $189.
Omega Engineering, www.omega.com

EDN ADVERTISER INDEX

EDN provides this index as an additional service. The publisher assumes no liability for errors or omissions.

 BY STEVE LUBS • DEPARTMENT OF DEFENSE

Too many cooks

DANIEL VASCONCELLOS

It started out as a simple design idea. I was designing a receiver for a TDM (time-division-multiplexed) data stream. The format was several blocks of 4 data bits each and then one block containing 5 bits, one of which was for synchronization. This pattern then repeated. My boss recommended a modified Johnson counter to handle the offset count. It worked perfectly.

After testing, I asked my boss whether he'd mind if I tried to publish it. He stared at me silently for so long that I thought he'd fallen asleep with his eyes open. Then he grinned. "OK" was his only reply.

Later that day, I handed him a three-quarter-page description plus a schematic and a timing diagram. He nodded, and said, "George has to sign off on it." George was my supervisor's boss.

George said he liked it. "But it needs some revising. Your description of the timing isn't clear," he added. "I sort of understood it. I don't think the readers will."

The other guys in the office got it, I thought. Who do you think reads the magazine? However, knowing my place in the food chain, I said, "What do you suggest?"

After 10 rewrites, which included almost a dozen "suggestions" and two face-to-face discussions, my simple article had grown to three pages of description with two added diagrams. George OK'd it, adding, "Now, all it needs is Ralph's signature." Ralph was George's boss.

I put it in Ralph's inbox, with a note. Ralph had a technical background, but he was primarily an administrator. He shouldn't do much more than look it over and sign off on it, right?

When I saw it again, red lines ran through half of my rewritten sentences, a red circle enclosed one diagram, and question marks and notes filled the margins. My supervisor stopped by my cubicle a couple of times and watched me rewriting and rewriting at my desk during lunch. Each time he left, he was grinning and shaking his head.

A month later, my article now two pages longer, Ralph OK'd my rewrite. "Now, have Security review it," he said, handing it back to me. "Can't I—skip them?" I asked. Ralph shook his head. Reluctantly, I stuffed the papers into an envelope and sent it. A month and a half later, I received a phone call. "Mr Lubs?" said the voice on the line.

"Yes?"

"I'm Hopkins, from Security. You wanted us to review an article you want to publish? About a Smith counter?"

My heart sank. "Yeah. Uh … it's a Johnson counter."

"Oh? Yes, I see." The voice paused. "The article is acceptable. Good luck publishing it."

"I … I … I … thank you, thank you, thank you, thank you," I said to the dial tone. I lost no time in sending the article to *EDN*. The editor sent me a draft to review before printing. When I saw it, I almost cried: It had been revised down to one page, a schematic, and a timing diagram. It looked very much like my original work. I wrote "Looks good" on it, sent it back, and saw it in print about three months later.

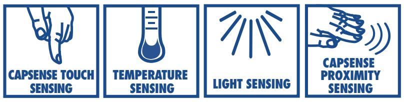
I've heard somewhere, "Too many cooks spoil the broth." What do you say when they aren't cooks, but they insist the broth needs fixing? I say it's my first big lesson in bureaucracy. I've had other big lessons. I'll tell you about them sometime. For now, though, I have a bunch more "broths" to fix. EDN

Steve Lubs has been an engineer in a variety of roles at the Defense Department for 30 years and has always argued with his bosses. Like Steve, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

It's showtime.

Get Your Ticket to the Ultimate Embedded Design Starter Kit.

Fixed-function microcontrollers had their share of the spotlight. It's time for a revolutionary—and simplified—approach to embedded application development. Get a Cypress PSoC® FirstTouch™ Starter Kit now and discover how much PSoC mixed-signal arrays—powerful, programmable analog and digital blocks, embedded memory and a fast MCU—shorten your time-to-market. This kit includes the easy-to-use PSoC Express™ visual embedded system design tool, and gives you embedded designs you can evaluate right out of the box. Get yours and step into the spotlight today.



Includes four ready-to-use mixed-signal applications on a single platform.

Buy your PSoC FirstTouch Ultimate Starter Kit now at:
www.cypress.com/go/FirstTouch

Buy Now
$29.95*

CYPRESS
PERFORM